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To Develop Efficient Layout of CMOS Circuit for SRAM and Compare with Existing Technique to Show the Proposed Technique is Efficient

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Abstract: Different SRAM cell typologies includes 10T, 9T, 8T, and 7T in performance improvement and stability that enhances in specific regions as a trade-of. The count of the transistors have the possibility to be reduces to compensate certain area with the dynamic CMOS logic utilization that have the possibility in high performance maintenance. The current research focused on a novel sleepy technique along with AVS design is proposed for low-power SRAM for reducing power consumption utilizing multi-threshold CMOS circuit. Therefore, the SRAM us implemented in the research using sleep transistors along with an additional leakage current feedback-transistor along with MTCMOS primary structure which is implemented with an effective results in terms of certain factors such as delay, area, and power.

Keywords: *SRAM, Leakage, Sleepy Keeper Transistor, Dynamic Power, CMOS design, PMOS design.*

I. Introduction

In the previous researches, miniaturization and performance of an associated device was considered as the main design issues, especially of a VLSI designer. Recently, a high-performance integrated circuits that are executed in deep sub-micron technology. There are plenty of previous researches has been carried out in the experimentation process with the portable devices development and design for emerging applications that includes space applications, wireless body-sensing networks, medical equipment implant, etc. Further, the utilization of scale-down in the node of technology, outcomes to enhance in the dissipation of static power. In order to reduce the leakage-power dissipation, different power reduction methods are used that includes leakage feedback, stack keeper along with body-bias, and sleepy keeper [2].

Moreover, the utilization of static RAM in embedded controllers needs minimum write and read time. Because of the significant enhancement of lower voltage and power on

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memory systems recently, SRAM [8] highlight in the certain research sector. The development of On-chip memory with the array that are tightly packed with the Static RAM cells that enables increased quality. A 6T-SRAM [10] has been used for a memory cell and the two types of power dissipation presented in an electronic circuit such as static power dissipation and switching power. In the time of performance on active mode during the device is under ON-state, hence the power dissipation is considered as a major process due to the semiconductor static components and switching power. With the execution of sleep or standby mode operation, the devices are found in the OFF state, for this the standby leakage current is considered as a responsible process for the dissipation of power. With the utilization of technology measuring the leakage power was commanding and the dynamic power, therefore is considered as a primary design issue to the VLSI designers, which was considered as that most of the devices that are portable with the battery operated [1].

While designing the low-power VLSI circuit, the dissipation of power is considered as one of the challenging problems that is integrated with threshold voltage. Therefore, the minimization of threshold voltage maximizes the sub-threshold current leakage with the leakage power-dissipation enhancement that plays a significant part in total dissipation of power. Because of the leakage power problem, certain devices that are executed by battery for a long period in the mode of standby that are drained-out fast. To reduce the issues on SRAM was developed with dual-control-stacked-inverter that exploits dual-control-signals [6].

The current research mainly focused on a novel sleepy stack technique with adaptive voltage scaling -AVS design development for low-power SRAM [9], [10] for minimizing power consumption utilizing multi-threshold CMOS circuit. The main contribution of the current research as follows: Section 2 explains the existing researches on low-power SRAM with the certain factors analyze and work process on different design metrics. Section 3 defines the proposed method for low power SRAM for reducing power-consumption using multi-threshold CMOS circuit. Section 5 explains the results and analysis with the power optimization methodologies and parameters. Finally, Section 6 explains the conclusion of the paper.

II. Literature Review

In [3], the research utilized an SEHF11T (11 transistors) processed on the SRAM cell with the high RSNM - read-static-noise-margin and write-static-noise-margin - WSNM. Therefore, the eradicates the write half-select-disturb utilizing cross-point-data-aware write-word-lines, that have the possibility to mitigate the structure of bit-interleaving to minimize multiple-bit-upset and maximizes soft-error immunity. This method has been analyzed and estimated with the PVT effect that defines temperature, voltage, and process variations on different design performance metrics when

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compared to the other cells. Further, the utilization of WSNM enhancement by eradicating the cross-coupled-inverters pair feedback while write operation that indicates the power-cutoff-write-assist method. Nevertheless, SEWA10T cell required more period to execute the read operation because of the decoupled-reading-buffer employment, developed by three series-connected-transistors.

In [4], KLECTOR - Keeper-in-Leakage-Control-Transistor has been used in the research to minimize leakage currents presented in SRAM architecture. This research focused on the SRAM impact on the leakage current in the "standby mode", that was processed by the fabric that minimize threshold voltage. Normally, KELECTOR circuit developed with minimum power consumption by limiting the current flow via devices of minimum voltage drops and completely dependent on the self-controlled transistor exhibited at the outcome node. It was denoted that the outcome on the static-leakage power in the write-operation, which was minimized to 63% & 69% executed for the operation (read). This design was experimented with the Cadence EDA, and Virtuoso tool.

In [5], the main focus of the research to include the procedures on current leakage-power procedures with a super low-voltage and low-power SRAM, that was executed using each method. By executing the analysis in memory cell, an unmistakable consideration was captured with the development of memory cells. This research utilized 16 x 16 SRAM array structure, which was developed utilizing SRAM, column decoder, address, and sense amplifier design. This research explained the SRAM cell design was have the capability to diminish the power dissipation leakage. The outcome obtained from the research with a 47.81% and 53.63% minimized in power dissipation in the absence of performance destruction executed in the array structure and memory-cell-level method. Possibly, the significant issues that are considered in the research are examined with the viable and new circuit execution method that minimized the power dispersal in the absence of circuit model compensation execution.

In [7], modified SRAM architecture has been utilized with minimum power dissipation. This research mainly concentrated on the utilization of 9T-SRAM-Cell to optimize a conventional SRAM with a single-bit-memory cell and therefore, designed a stable procedure along with low-power consumption and achieved low PDP - Power-Delay-Product by differing executing frequency measured in range of MHz. Further, a 4x4 SRAM array was executed with the comparative analysis amidst 9T-SRAM cell and 6T-SRAM cell with the minimization of power at 62.83% acquired in this system with the previous system at a 2GHz operating frequency. This paper defines a 62.27% power reduction was acquired for the structure of array and the single-bit 9T PDP - power-delay-product and power dissipation which was lesser, when compared to the conventional 6T-SRAM. Also, this research implemented with the utilized method of SRAM to an array with the connecting peripherals. Here, used a forced sleep method,

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which was a combination of sleep effect and forced stack method. While using the sleep transistor method in the existing research, PMOS was coupled amidst Vdd and pull-up track. Nevertheless, NMOS was coupled amidst ground and the pull-down track, at the same time in using the forced sleep method, the connection applied was reversed.

III. Proposed Methodology

The current research focused on a novel sleepy technique along with AVS design is proposed for low-power SRAM for reducing power consumption utilizing multi-threshold CMOS circuit. Therefore, the SRAM us implemented in the research using sleep transistors along with an additional leakage current feedback-transistor along with MTCMOS primary structure which is implemented with an effective results in terms of certain factors such as delay, area, and power. Therefore, the power dissipation of dynamic and static power with the delay formed by sleep transistors are substantially minimized when the sleep transistors development such as leakage-current-feedback-transistor addition. As a next step, the power optimization has been utilized in the research that performs to minimize package cost and to broaden batter life to minimize SRAM circuit power dissipation (total). Finally, effective layout has been developed and designed for SRAM circuit and COMS to minimize the area than existing method.

3.1 Conventional SRAM:

The conventional SRAM used in the research helps to store binary data (1 bit) with the SRAM [12] cell development, that utilizes a bi-stable-latching-circuitry. Therefore, the memory cell used in the research defined with the 2 stable states that denoted as 1 and 0. The 2 inverters circuits used in the research are integrated with the cross coupled mutually. After this, 2 more NMOS transistors that defined as Cnt_N is used in the process that control access, especially in the storage cell while executing both write and read operations. Further, gate terminal control transistors are interconnected to the operation signal (both read & write) WL - Word Line and six MOSFET has been used to store cell data in memory with the typical SRAM. When WL runs high, control-access transistors tend to be turned ON, especially for write operation. Here, two complementary bit-lines including BL and BLB are used in the operation with the cell connection with the data transcribed in memory cell. However, SRAM-cell is inaccessible from bit lines (both), after this the SRAM settled in standby mode with the unchanged stored value. Fig 1. represents the conventional SRAM and Fig.2 defines the transient waveform.

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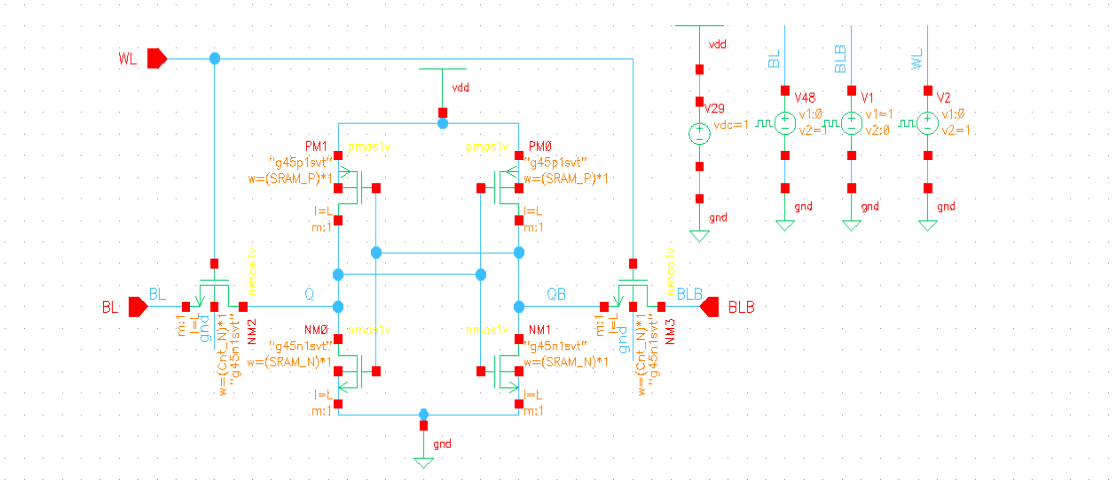

Figure 1 - Conventional SRAM

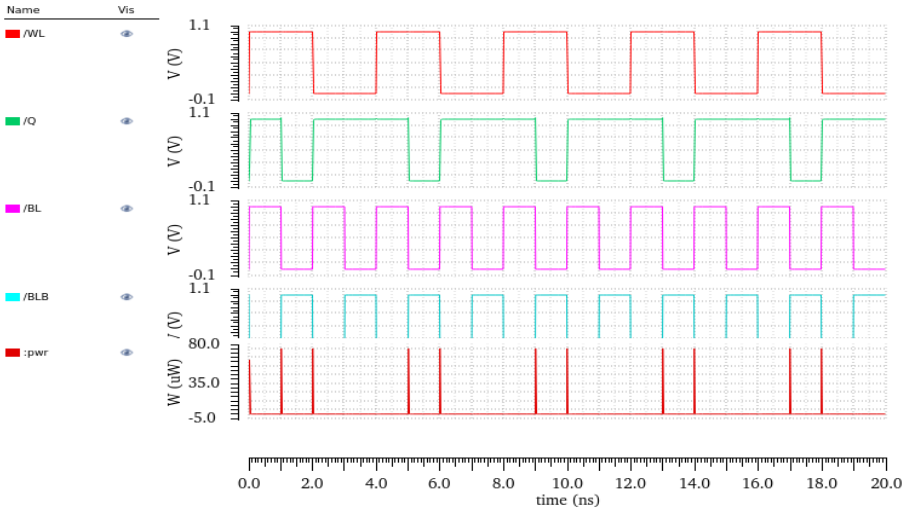

Figure 2 - Transient Waveform

3.2 Sleepy SRAM:

The sleepy SRAM executed with the circuit level methods that are performed earlier for minimizing sub-threshold-leakage-power method, which is a sleepy method. Therefore, the technology on sleepy SRAM utilizes sleep transistors in two places which has different phases. The pull-up network presented amidst Vdd (ST_P) and pull-down network presented amidst (ST_N) and Gnd. Here, the size of sleep transistor is provided, which is relative to either pull-down or pull-up transistor interconnected to the sleep transistor and the sleepy SRAM represented in Fig 3.

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3.2.1 Active Mode

In the active mode state, the sleep signal represented as slp indicates the logic 1 with complementary sleep signal represented as slpb and voltage level, represented logic 0 with voltage level. Further, the sleep transistors (ST_P, ST_N) represented in active mode are ON. In the execution, when the power provided to the circuit with the sleep transistors turned ON with the outcome node on VP defined at VDD with the VG node presented at ground potential.

3.2.2 Sleep Mode

In the execution of sleep mode with the sleep signal represented as slp denoted with logic-0 with complementary sleep signal and voltage level slpb that defined the logic-1 voltage level. The sleep transistor denoted as ST_N and ST_P which are on the OFF state. Because of this reason, the ground and supply are isolated from the logic-circuit. Eventually, the static-power is set as virtually 0. Because of the effect on stack, the off-resistance increased with the minimization of leakage current. The technique generates state destruction with the floating voltage output, however, the outcome procured with the floating values after sleep mode. Addition of sleep transistors enhances the delay as well as area. In case of WL - word line raises high, the control-access transistors are in the position of ON condition, especially in the writing operation. Therefore, there are two complementary bit-lines that includes BL and BLB are interconnected to the cell, and the data obtained are written in the proper cell memory. In certain stage, SRAM cell is inaccessible from bit lines, while it was in standby mode. Here, the stored value sustains in unchanged position with the suppressed leakage current. These functioning are represented in Figure 3.

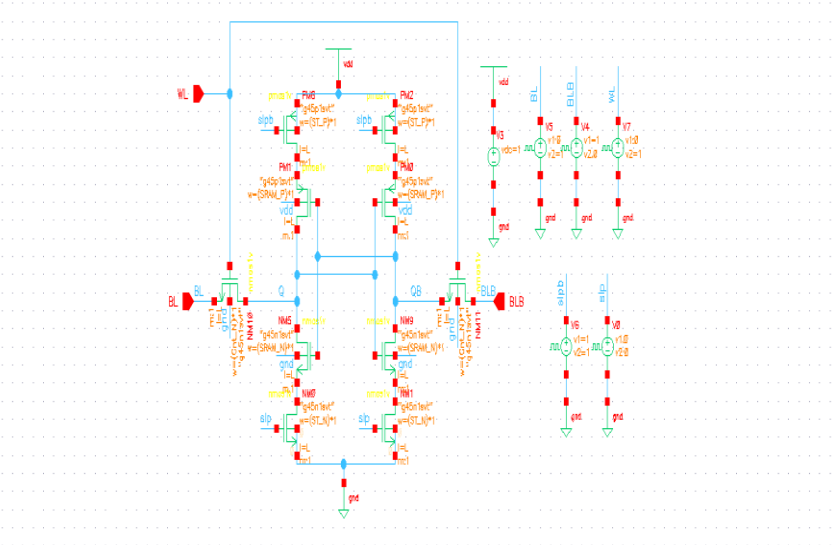

Figure 3 - Sleepy SRAM

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3.3 Stack SRAM:

The stack method has been utilized in the research, which is considered as the another low-power-reduction strategy. Normally, it segregates the present transistor into 2-pieces and the transistors which was duplicated enable little reverse bias amidst the source and gate during the 2 transistors was in the OFF position (turned off) simultaneously. Because of the sub-threshold present dependency processed on gate bias with enhanced area and delay, obtained with a significant current minimization. Probably, certain execution resolves sleep method's limits with the help of maintaining state, however it enhances wake-up time. Eventually, the SRAM logic state circuit is also can be retained. Figure 4 represents the Stack SRAM Inverter.

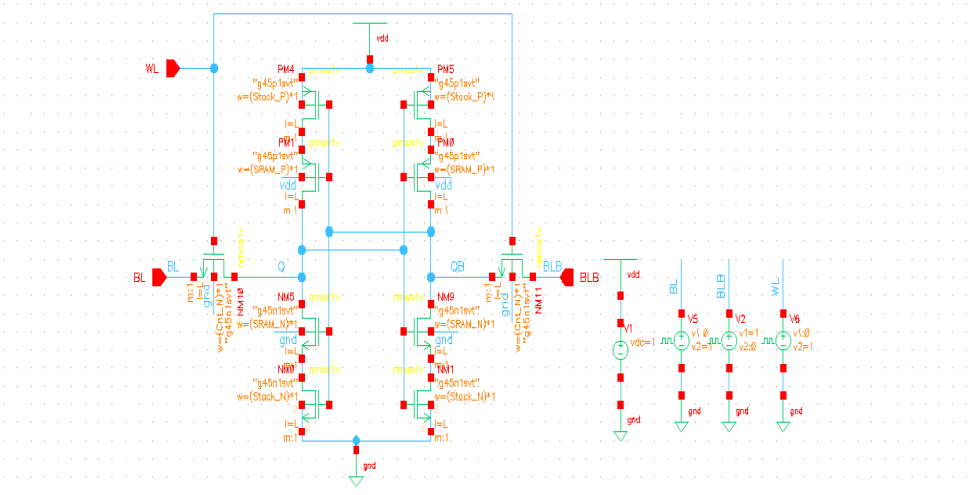

Figure 4 - Stack SRAM Inverter

3.3.1 Sleepy Keeper SRAM

This approach holds the sleepy method circuits maintain similar and in-addition with the P_MOS that defined as ST_P_K and N_MOS that defined as P_MOS transistors, that are combined in parallel amidst vdd, pull-down and pull-up network with gnd. Therefore, the effective way to utilize the CMOS transistors and PMOS, that are interconnected to NMOS and Vdd connection to gnd. At the same time, the NMOS transistors in the process are widely known for becoming ineffective at shifting Vdd and the PMOs-transistors are widely known for becoming inefficient at shifting Gnd. Certain floating voltage output has been surmount with the introduction of sleepy-keeper method. In case of sleep-mode, the ST_P sleepy PMOS-transistors has to be turned OFF with the N_MOS transistors (ST_N_K) interconnected amidst oull-up n/w and VDD that holds specific data that represented as "1", which is turned "ON". Likewise, in order to turn "ON" the P_MOS-transistor with the data holding '0', that are interconnected amidst the GND and pull-down N/W with the ST_N sleepy NMOS-

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transistor to turn in the state “OFF”. Hence, this enables to keep the specific data utilized in the process are safe, especially in sleep or standby mode. During the WL drives high with the turned “ON” position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 5 & 6 represents the Sleepy Keeper SRAM and transient waveform of it.

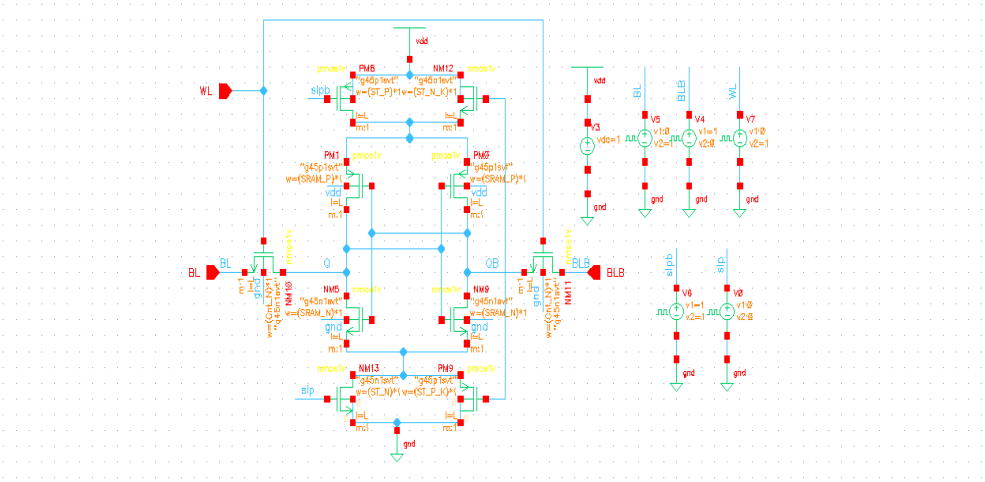

Figure 5 - Sleepy Keeper SRAM

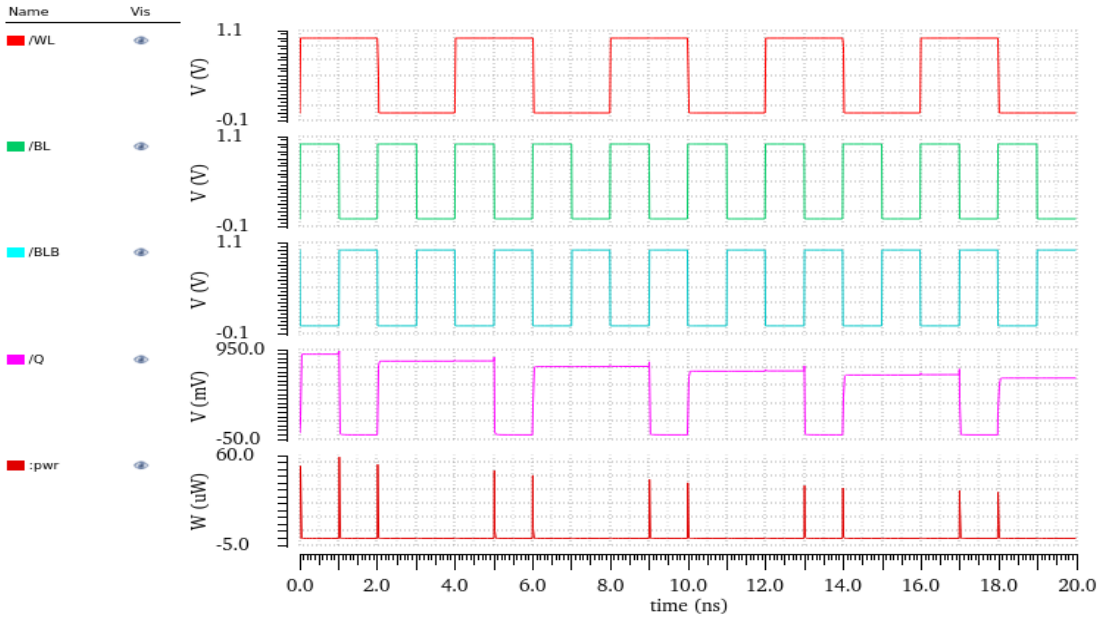

Figure 6 - Transient Waveform for sleepy Keeper SRAM

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3.4 LECTOR SRAM

The main theme of using this method is to enhance the transistor number in the "OFF" state in the gnd path and source. Therefore, the 2-leakage control transistors that includes NMOS (LCT_N) and PMOS (LCT_P) interconnected amidst pull-down and pull-up network. The PMOS gate terminal is interconnected to empty the SRAM_N pull-down network, which is interconnected to empty the SRAM_P pull-up network. The PMOS body terminal is interconnected to Vdd and NMOS is interconnected to gnd. In the process of sleep-mode, the selection of NMOS transistor or PMOS transistors(any one) should be in the "OFF" state or close to cut-off area. Normally, this raises the path in resistance amidst gnd and Vdd and this method, also minimized the leakage power. Hence, the LCT-transistor size is optimized in the research for effective outcome and the enhancement of dynamic power with the SRAM static-power is minimized.

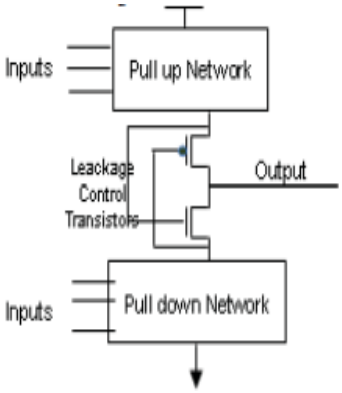

Figure 7 - Process of LECTOR SRAM

During the WL drives high with the turned "ON" position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 7 indicates the process of LECTOR SRAM and Figure 8 & 9 represents the LECTOR SRAM and transient waveform of it.

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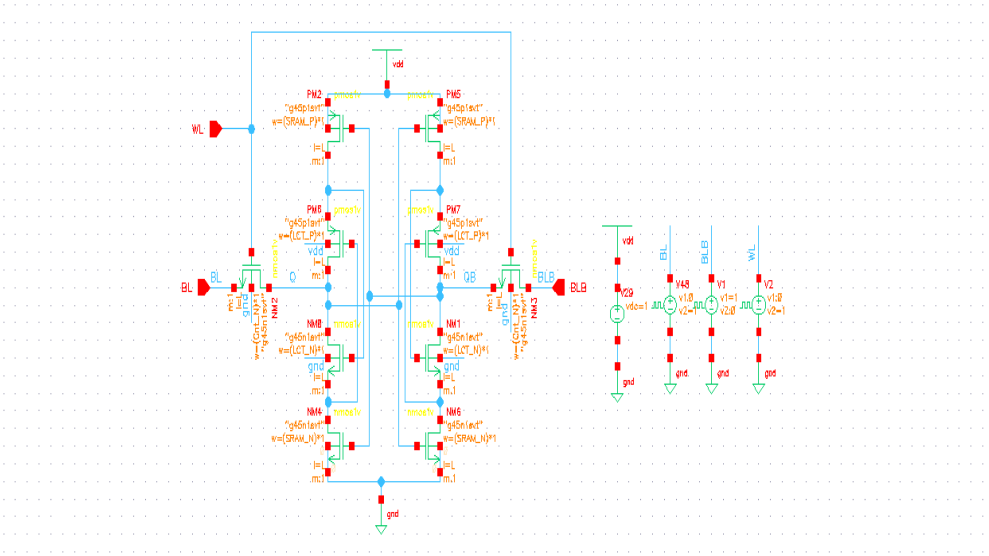

Figure 8 - LECTOR SRAM

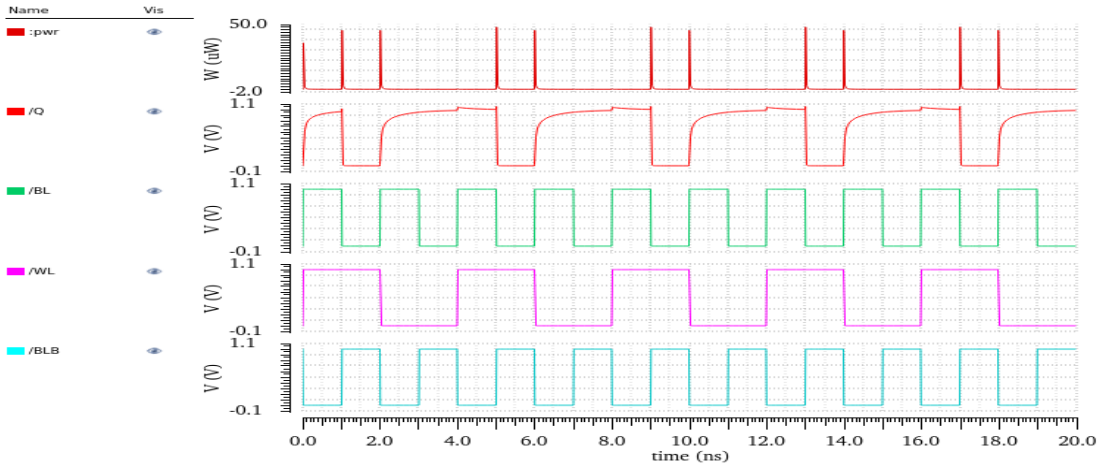

Figure 9 - Transient Waveform for LECTOR SRAM

3.4.1 Sleepy Keeper LECTOR SRAM

This method are processed with a combination of LECTOR and sleepy keeper method. During the process of sleep mode with the sleepy transistor represented as ST_P and ST_N, which are turned OFF. Therefore, the parallel transistors includes ST_P_K and ST_N_K that helps in holding the data in sleep-mode that reduces the leakage power and the power minimization done by LCT_N and LCT_P due to the multiple transistors in sleep mode and "OFF" state that enhances the resistance path amidst gnd and vdd. During the WL drives high with the turned "ON" position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory

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cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 10 & 11 represents the Sleepy Keeper LECTOR SRAM and transient waveform of it.

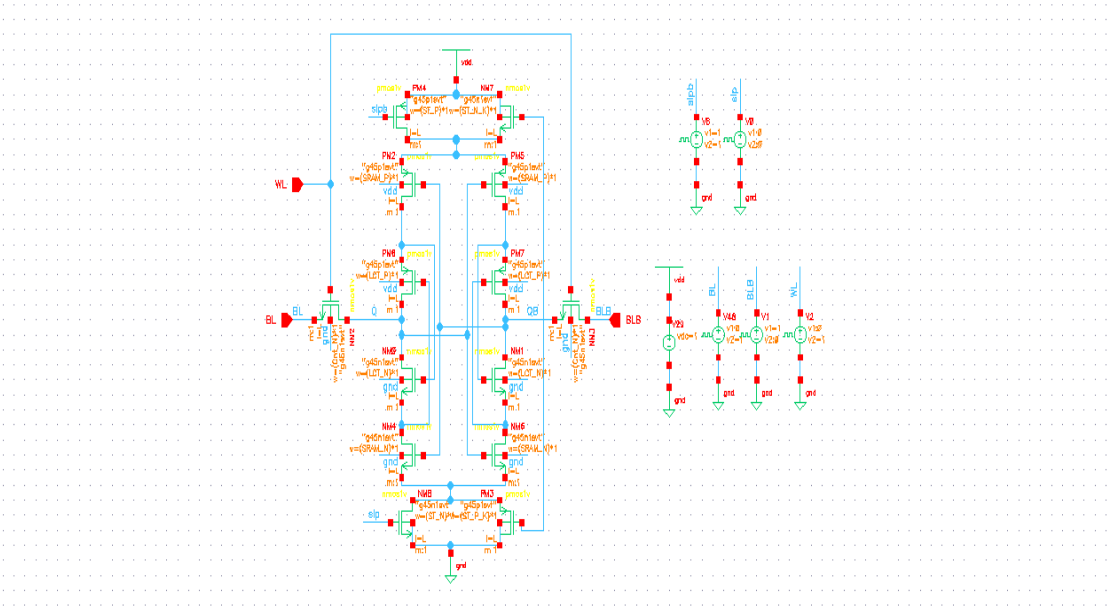

Figure 10 - Sleepy Keeper LECTOR SRAM

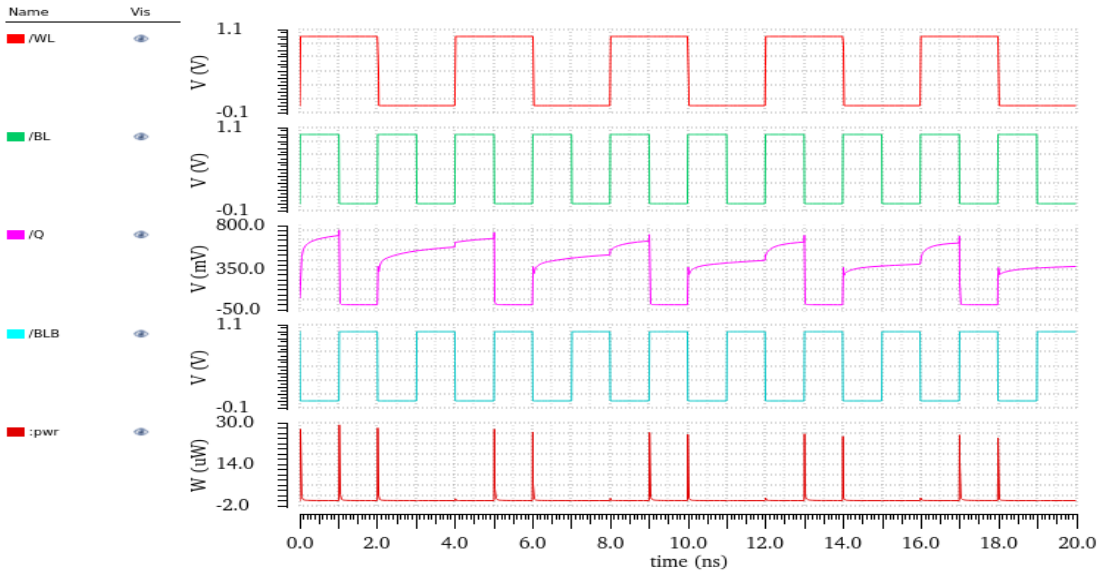

Figure 11 - Transient Waveform for Sleepy Keeper LECTOR SRAM

3.4.2 Sleepy Stack SRAM

The sleepy stack SRAM [11] structure used in the research defines a novel technique that minimizes leakage power with the integration of the sleep and stack transistor

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structure. Here, the sleep stack method has 2-modes that define as first and second mode in sleep condition. By using a forced stack method in the research, the previous transistors used are split into 2-transistors with the benefits of stack structure from the effect of stack. On the other hand, sleep transistors are placed parallel to a transistor (stacked) to achieve state retention and low-power leakage by integrating these techniques.

3.4.2.1 Active Mode

In the Active Mode, the sleep transistors are in "ON" state of the sleepy-stack transistor. Therefore, this mode have the possibility to allow for circuit delay minimization and all the presented sleep transistors are in "ON" state, in the mode of active that outcomes in a rapid switching time. During the process of transistor, which is parallel to sleep-transistors, the voltage of threshold value may be attained to high.

3.4.2.2 Sleep Mode

In the sleep-mode, the transistors are disabled with the preservation of precise logic state using the structure of sleepy stack. It is noted that the sleep transistors are being in a state of "OFF" that results in the effect of stack, that minimizes leakage power consumption. Utilizing the sleep stack method enhances the speed in different ways during the sleep transistor on the state of "ON", and current flows via the circuit. Hence, it is significant to switch circuit speed and it is enhanced with the minimized delay.

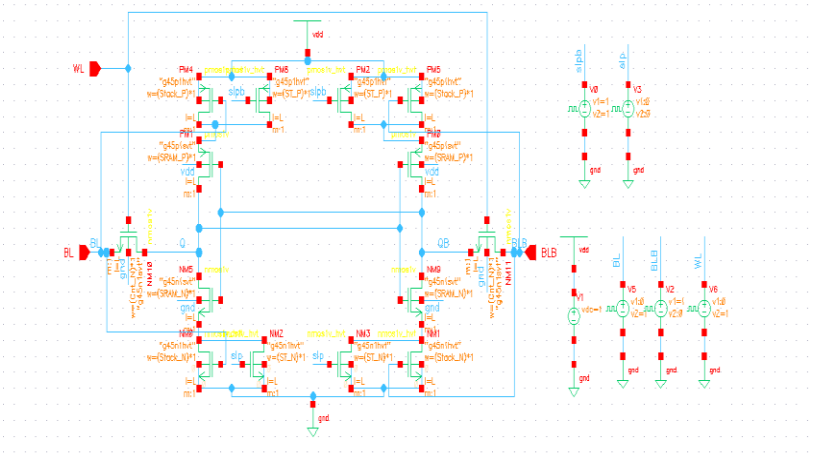

Figure 12 - SRAM block using Sleepy Stack Technique

3.5 SNM (Static Noise Margin)

The memory cell stability has been acquired in the noise presence is evaluating utilizing static noise margin. Therefore, it can be featured with the lowest-voltage that should be enabled to store nodes for a certain state to flip. There is a possibility to measure SNM by including the voltage transfer features of the 2-inverters that imparted in the memory

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cell. Further, the inverters of memory cell's are developed to manage stable states with the output nodes includes the data that is stored in the memory. Further, the node voltages initialized varying due to the noise presented at the storage nodes that results in a cell stability decline of 55. The utilization of SNM evaluates the maximum permit level of noise voltage with the capability of these inverters management with their current state in the noise presence.

Moreover, employed an advanced low-power processors with DVS - dynamic-voltage-scaling, which is considered as a feasible option, especially for power reduction. With the help of the DVS, the operation of system is executed in the highest frequency at the specific supply VDD and VDDnom that defines nominal supply-voltage. Therefore, it can be operated in low power-mode at the scaled-VDD. The significant utilization of supply voltage, which is minimized than its value at nominal stage in the scheduled tasks completion with the minimum energy usage amount.

In the modern digital VLSI-systems [14] along with the utilization of SRAM cells that share a substantial portion, that have the similar supply-voltage with the other processing units. Therefore, since the another digital components that are executed at their lowest energy-point with the continuation of SRAM that operates with reliability at specific scaled VDD. The different stages such as M1, M2, M3, M4, M5, M6, and M7 that defines Conventional Technique, Sleepy SRAM, Stack SRAM, Sleepy Keeper Technique, LECTOR technique, SK-LCT technique [13], and Sleepy Stack SRAM.

IV. Results And Discussion

The current research focused on a novel sleepy technique along with AVS design is proposed for low-power SRAM for reducing power consumption utilizing multi-threshold CMOS circuit. In the part of power dissipation, it has been analyzed with the PDP - Power-Delay-Product - PDP, Leakage-current, Energy-delay-product - EDP, and PEP - Power-Energy-Product, duty-cycle, and Clock Frequency. The layout of the developed schematic for existing design has been mentioned in the research previously. The parameter used in the research such as Area (μm), tpdf (ps), tpdr (ps), propagation delay tpd (ps), Static power (W), dynamic power NMOS (W), dynamic power PMOS (W), power (J), energy (J), PDP (J), PEP (J), EDP (J), clock frequency (Hz), and duty cycle (Q) on power optimization methodologies such as M1 (con), M2 (sleepy), M3 (stack), M4 (SK), M5(LEC), M6(SK_LEC), and M7 (SS-hvt transistor) represented in Table I. Here, in the current research, figure 13 represents the layout of the conbf, the conventional technique.

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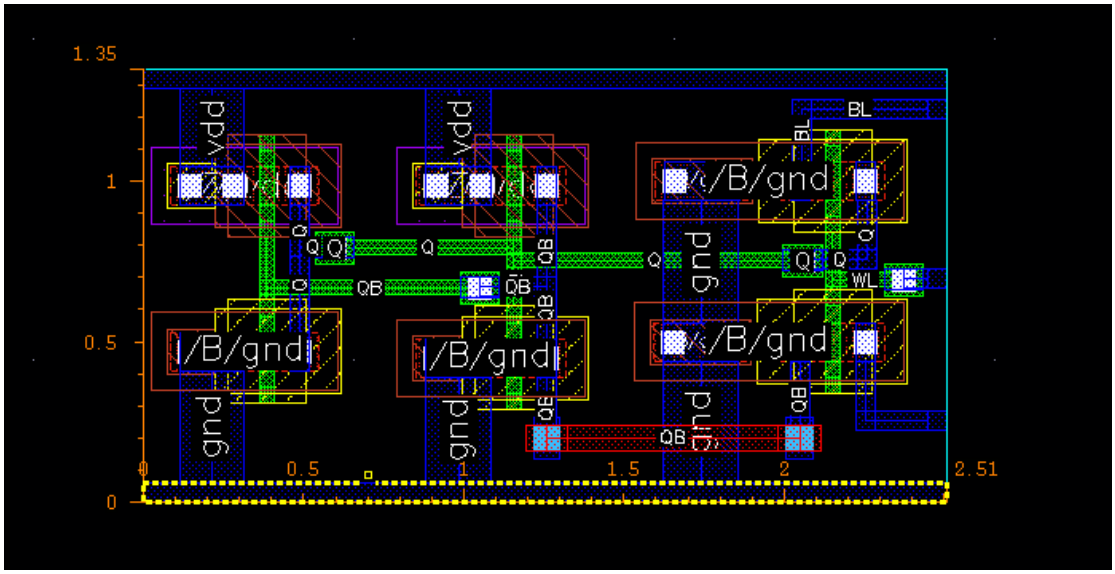
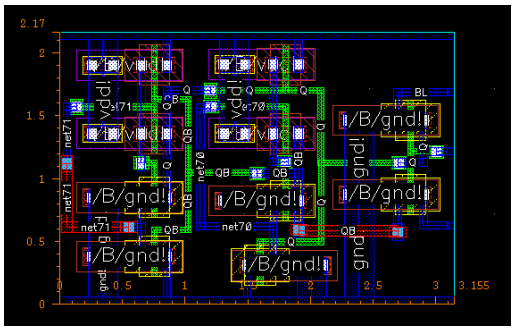
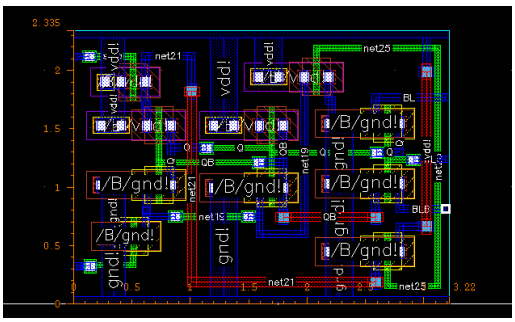


Figure 13 - Layout of the Conventional Techniques

The layout of the LEC, SK, SK_LCT, sleepy layout, sleepy stack, and stack has been denoted in the simulation process in figure 14 a, b, c, e, f, g, and h.



(a)



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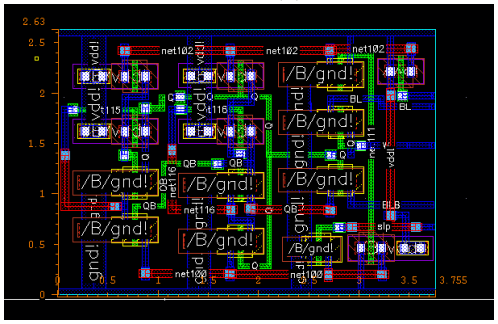

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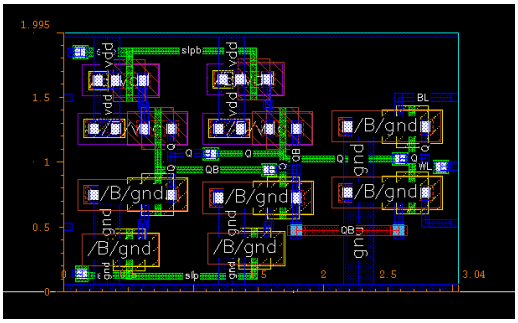

(d)

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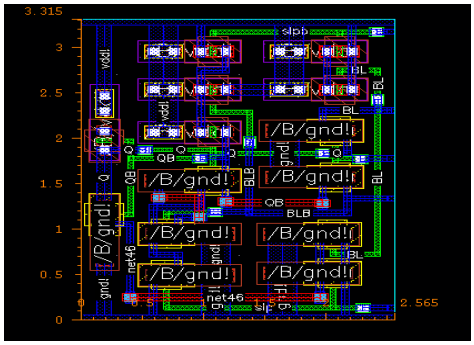

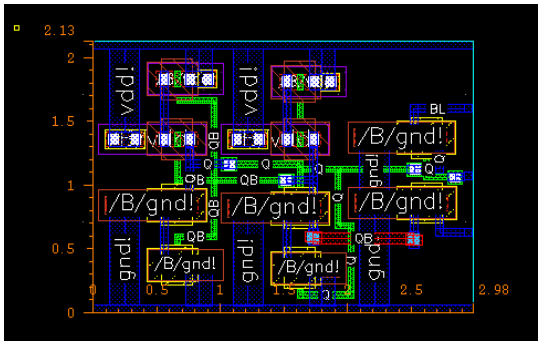

SL. No	Parameter	Power Optimization Methodologies						
		M1 (con)	M2(sleepy)	M3(stack)	M4(SK)	M5(LEC)	M6(SK_LEC)	M7 (SS-hvt transistor)
1	Area (µm)	3.3885	6.0648	6.3474	7.5187	6.8464	9.8757	8.502975
2	tpdf (ps)	10.882	5.874	7.454	5.536	5.642	4.436	5.833
3	tpdr (ps)	28.306	26.660	28.264	29.796	29.979	49.648	11.228
4	Propagation Delay tpd (ps)	19.594	16.267	17.859	17.666	17.810	27.042	8.530
5	Static Power (W) Vin=0V	2.381 E-6	76.148E-12	712.94 E-12	43.481 E-12	1.036E-6	42.503E-12	146.87 E-12
6	Static Power (W) Vin=1V	1.427 E-6	35.13E-12	421.81 E-9	26.641 E-12	5.633E-9	25.318E-12	9.154E-12
7	Dynamic Power (W) NMOS	13.559E-9	30.364E-12	2.417E-9	45.246 E-12	459.26 E-12	11.990E-12	40.709 E-12
8	Dynamic Power (W) PMOS	133.29E-9	167.874 E-12	29.047 E-9	192.56 E-12	47.855 E-9	111.554E-12	206.854 E-12

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9	Power (W)	1.041 E-6	363.603 E-9	651.24 3E-9	363.37 8E-9	526.87 E-9	220.169E-9	336.64 E-9
10	Energy (J)	2.560 E-15	601.591 E-18	1.513E-15	450.56 E-18	1.511E -15	445.682E-18	354.708 E-18
11	PDP (J)	20.40 E-18	5.914E-18	11.630 E-18	6.419E -18	9.383E -18	5.953E-18	2.871E-18
12	PEP (J)	2.665 E-21	218.741 E-24	985.96 6E-24	163.72 E-24	796.17 E-24	98.125E-24	119.409 E-24
13	EDP (J)	50.17 E-27	9.786E-27	27.038 E-27	7.959E -27	26.914 E-27	12.052E-27	3.025E-27
14	Clock Frequency (Hz)	500M	500M	500M	500M	500M	500M	500M
15	Duty Cycle Q (%)	69.73	69.53	69.64	69.48	69.88	41.69	74.98

(e) (f)

Figure 14 - (a) LEC (b) SK (c) SK_LCT (d) Sleepy layout (e) Sleepy Stack & (f) Stack

Table I - Comparison of proposed work with the Existing Researches with the Power Optimization Methodologies based on parameters

This research also compared with the parameters in the research such as Area (μm), tpdf (ps), tpdr (ps), propagation delay tpd (ps), Static power (W), dynamic power NMOS (W), dynamic power PMOS (W), power (J), energy (J), PDP (J), PEP (J), EDP (J), clock frequency (Hz), and duty cycle (Q) on power optimization methodologies such as M1 (con), M2 (sleepy), M3 (stack), M4 (SK), M5(LEC), M6(SK_LEC), compared with M7 (SS-hvt transistor) represented in Table II with increment and decrement values. The inc represents the proposed value increased compared to existing method and dec represents the proposed method value decreases compared to existing method.

4.2 Comparison table on Parameter with the value increment and value decrement on M1, M2, M3, M4, M5, and M6 with M7

SL. No	Parameter	M1 vs M7		M2 vs M7		M3 vs M7		M4 vs M7		M5 vs M7		M6 vs M7	
1	Area (μm)	60.15	inc	28.67	inc	25.35	inc	11.58	inc	19.48	inc	16.14	dec
2	tpdf (ps)	86.56	dec	0.70	dec	27.79	dec	5.09	inc	3.27	inc	23.95	inc

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3	tpdr (ps)	60.33	dec	57.88	dec	60.27	dec	62.32	dec	62.55	dec	77.38	dec
4	Propagation Delay tpd (ps)	56.47	dec	47.56	dec	52.24	dec	51.72	dec	52.11	dec	68.46	dec
5	Static Power (W) Vin=0V	99.99	dec	48.15	inc	79.40	dec	70.39	inc	99.99	dec	71.06	inc
6	Static Power (W) Vin=1V	100	dec	73.94	dec	100.00	dec	65.64	dec	99.84	dec	63.84	dec
7	Power (W)	67.66	dec	7.42	dec	48.31	dec	7.94	dec	36.11	dec	52.90	inc

V. CONCLUSION

The current research focused on on a novel sleepy technique along with AVS design is proposed for low-power SRAM for reducing power consumption utilizing multi-threshold CMOS circuit. Here, a high speed and low-power SRAM architecture was developed utilizing Conventional Technique, Sleepy SRAM, Stack SRAM, Sleepy Keeper Technique, LECTOR technique, SK-LCT technique, and Sleepy Stack SRAM. The modern digital VLSI-systems along with the utilization of SRAM cells that share a substantial portion, that have the similar supply-voltage with the other processing units. Therefore, since the another digital components that are executed at their lowest energy-point with the continuation of SRAM that operates with reliability at specific scaled VDD.

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