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Design of Voltage Level Shifter with Wide-Range Conversion for Multi-Supply Design Applications

T. Jaya Chandra prasad[1], M Chennakesavulu[2], K. Deveswar Reddy[3], K. Ruchitha Reddy[4] B. Venkata Sushma[5] C. Hema vardhan[6]

[1,2]Department of ECE
RajeevGandhiMemorialCollegeofEngineering&Technology,Nandyal,India,518501
[3,4,5,6]Department of ECE
RajeevGandhiMemorialCollegeofEngineering&Technology,Nandyal,India,518501
Corresponding author: chennakesavuluece@rgmcet.edu.in

Abstract:-

This paper introduces a high-efficiency, minimal power, and rapid voltage conversion over a wide operating range level shifter. The circuit comprises leakage suppression transistors to eliminate standby power dissipation. For improved switching speed, a LVT is employed in the pull-down network, thereby providing a fast fall transition. A threshold voltage hysteresis transistor also improves the pull-up stage, which aids in the fast and full charging of internal nodes, thereby addressing signal swing issues. The circuit is performed at schematic level in a 45nm process, and experimental results show an average power of 1.04nW when it is converting from 200mV to 1.2 V. the level shifter has an average signal delay of 17.77 ns transition. And the proposed circuit have better efficiency 87% compared with remaining existed methods. The circuit achieves voltage transforms from 200mV to 1.2 V, thereby making it especially well-suited for low-power applications and multi supply voltage systems.

Keywords: — Level Shifter, Ultra-Low Leakage, Voltage Conversion, Low-Power Design, Propagation Delay, multi -supply design

1. Introduction

WITH the advancement of compact electronic devices like smartphones and personal computers, power consumption minimization in digital circuit design has been the foremost priority. operating voltage minimization is one of the most optimal strategies of system power usage minimization. Lower supply voltage, however, that it compromises the circuit speed. To get a balance between power efficiency as well as performance, multi-voltage technology is utilized, and different functional blocks are designed to operate at various voltage levels. In such system networks, level shifters (LS) play a crucial role in achieving seamless voltage conversion between distinct voltage domains.

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Delay time, power usage and power delay product are the three most significant performance metrics of a level shifter.

With the difficulty of the System-on-Chip (SoC) design increasing, high-speed as well as low-energy consumption level shifters are being increasingly required in low-power designs.

Basically, we have a three mostly used topologies in level shifters. In that the differential cascade voltage switch levelshifter (DCVSLS), which is marred with conflict between the pull-up structure network and pull-down structure network. The contention aggravates when the supply voltage falls in the sub-threshold region, which results in voltage level shifting failure. current mirror level shifter (CMLS) is one of the level shifters traditional designs. Though this structure reduces contention when compared to DCVSLS, the pull-up network is weaker. Also, with partial switching of transistors, this design adds extra static power consumption. Wilson current mirror level shifter (WCMLS)

By using WCMLS we have a different LS structure [3], [4], [5], [6], [7], [8], [9]. It has self-controlled current limiting to reduce pull-up strength, a reduced swing buffer to reduce static current, and a pass transistor to minimize transition delay. However, low voltage swing might degrade signal integrity and increase static power in the next-stage buffer [3]. A Wilson current mirror with reflected-output further improves the power efficiency with area reduction of not requiring any large-sizing-ratio current mirror. However, static power increase may occur at the next stage with lower output swing, which could degrade its performance at extremely low voltages[5].The energy efficiency and low static power characteristics of the combined-threshold current mirror are achievable through additional bias circuits, even though voltage drop at internal nodes might limit its conversion range and speed[6].A auto-biased minimal voltage cascade current mirror with a segmented-input inverting buffer improves energy efficiency and speed, but suffers from higher static power consumption, and delay may degradation due to aging over time[7].The circuit has integrated the head PMOS as well as the cut-off and has a low-to-high error correction circuit that helps in eliminating static current and thus improves its speed but reduces output swing, which may later increase static power in the next-stage buffer[8].Static current elimination and improvement in voltage conversion are done with the help of an error checking logic circuit and an enhanced current mirror structure, but this yields higher contention at lower supply voltages and higher circuit complexity[9].

This paper introduces a new current mirror-based level shifter (LS) that uses a voltage hysteresis transistor to minimize internal node voltage swing. The use of mixed-threshold transistors reduce contention and help in enhancing the delay along with the voltage conversion. A shut off leakage transistor controls the leakage current to ensure it is as low as

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possible. The proposed LS utilizes design strategies that are innovative enough to attain very less power consumption and rapid speed voltage conversion. The brief is divided in this way: Section II Describes the proposed LS; Section III reports the measurement outcomes and comparisons; Section IV conclusion and summarizes the study.

2. Design of Voltage level shifter

A. Proposed voltage level shifter

With a novel current mirror technique, the proposed voltage level shifter circuit introduces and also consists an output buffer to increases the speed and reduces consumption of power in the circuit. Table-1 shows the size of the transistors for the proposed voltage level shifter, and figure-1 shows the proposed design of the optimized voltage level shifter.

TABLE-I TRANSISTOR OF PROPOSED VOLTAGE LEVEL SHIFTER

L(nm)/W(nm)	PMOS Transistor	L(nm)/W(nm)	NMOS Transistor
400/120	MPO	120/200	MNO
200/150	MP1	180/120	MN1
70/120	MP2	200/120	MN2
120/300	MP3	120/80	MN3
90/120	MP4	60/130	MN4
80/120	MP5	60/120	MN5
100/120	MP6	80/120	MN6

A LVT transistor MN4 is employed to get a high-speed pull-down network in order to speed up the pull-down of node Q2 and minimizes transmission delays. This will help to quickly discharge node Q2, thus improving the response time of the circuit. Especially in the operation of the pull-up network. To assure that the current mirror under consideration is switched off in time when node Q2 is charged completely, a transistor MN2 is used. This shuts off the current mirror when it is no longer in use, thereby saving energy and preventing power consumption in the circuit

As the supply voltage goes from low voltage to high voltage, the circuit switches on the low-threshold transistors MN0 and MN1, enhancing the pull-down network. MN0 and MN1

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ensure they are switched on, and the internal node Q2 will charges by the current mirror through transistor MP1. Although, as the supply voltage approaches or enters the sub-threshold region, the pull-down network formed by MN0 and MN1 becomes insufficient to discharge node Q1 and it will take a more time to charge node Q2. This will reduce a voltage swing, and idle current produced in the subsequent stage buffer will be more.

To overcome that problem, here used a hysteresis-controlled voltage transistor MP2 is used for the decrease the pull-up strength of MP0. The node Q1 sees a reduced voltage swing, ensuring that node Q2 charges faster. With MP2 in the circuit, node Q2 charges faster at the expense of MP1 due to the improved swing it offers. In addition, the voltage supply is source of transistor MN4 so that MN4 is fully turned off and prevents any leakage of current. This ensures that no unnecessary power is lost in the circuit during its operation.

And the circuit have a leakage control transistor, MN2, for the further optimization. When node Q2 is high and transistor Q3 shifts to low, MN2 is turned off, by closing the current mirror and stopping any current flow. This will not only be minimizing consumption of power but also maintain the overall energy-saving operation of the circuit. All of these components were integrated to overcome the reduced swing problem, to improve the charging speed of the nodes, and to minimize the leakage currents to make it an efficient and power-optimized circuit.

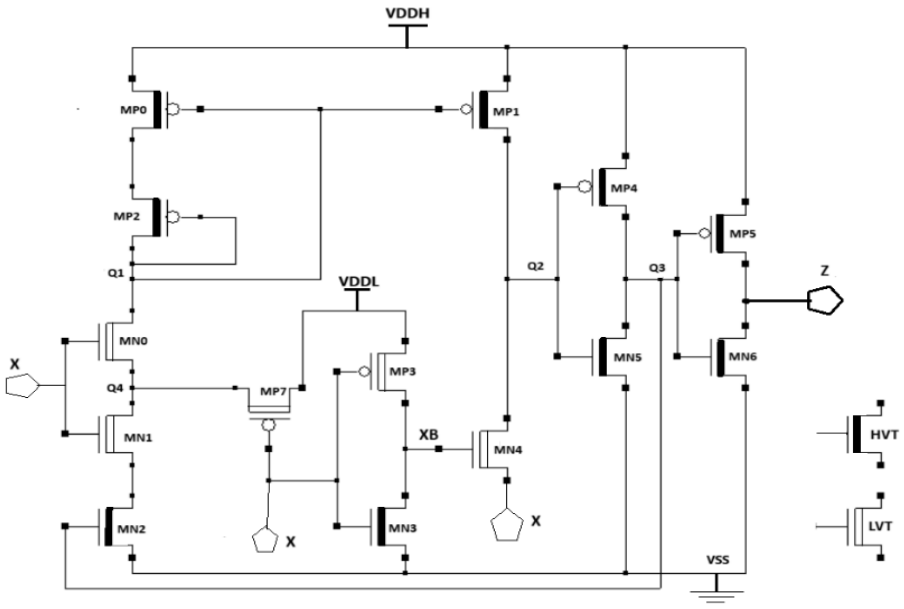

Fig -1:CIRCUIT REPRESENTATION OF PROPOSED VOLTAGE LEVEL SHIFTER AT SCHEMATIC LEVEL

when the supply voltage will change from high (VDDH) to low (VSS), the transistor MN4 will be ON. This turns node Q2 into a low voltage (VSS) with a quick discharge, that will be ensuring that node Q2 goes into its low state. The idle current of the novel current mirror is

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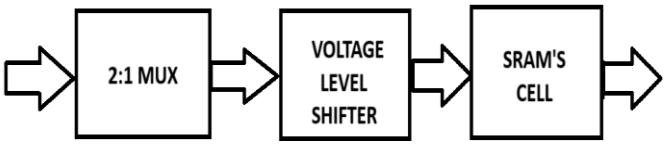
controlled when the supply voltage is low by the voltage at node Q4 in terms of leakage current. With the voltage at node Q4 reaching VDDL, the leakage current will be reduced. For reduce some effect, a threshold hysteresis voltage transistor MP6 is included in the circuit. MP6 increases the voltage at node Q4 between MN0 and MN1 to strengthen the shut-off of the NMOS transistors and completely turn off the current mirror.

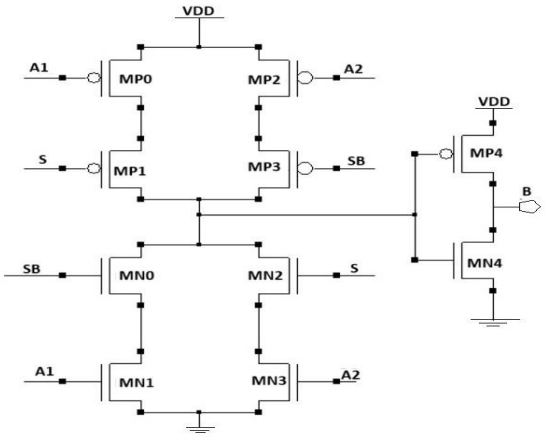
By adding MP6 will leads to additional power consumption in the circuit, it will be reducing the leakage current, which is very much better than in a regular design that doesn't include such a feature. This results in a greatly improved overall power efficiency. Simulation results indicate that although the circuit consumes a very small amount of additional power because of MP6, the overall power consumed by the circuit is significantly less than in conventional stacked NMOS configurations, and hence the proposed design is effective in reducing power loss and optimizing energy consumption.

B. Multi-supply Design Application

This proposed voltage level shifter design is verified to work as expected by testing it in a multi-supply application. Theapplication transfers the lower-voltage output from a multiplexer to a static RAM that operates with a higher supply voltage. In this configuration, the multiplexer runs at 200mV, but the SRAM runs at 1.2V. Because these two modules cannot directly communicate because of a voltage mismatch, the level shifter is introduced between them. The level shifter converts the 200mV output from the multiplexer to up-convert SRAM, and it stores this signal. Figure-3 will illustrate the block diagram of the multi-supply design application and in detail it will explains in the remaining sections.



(a)



(b)

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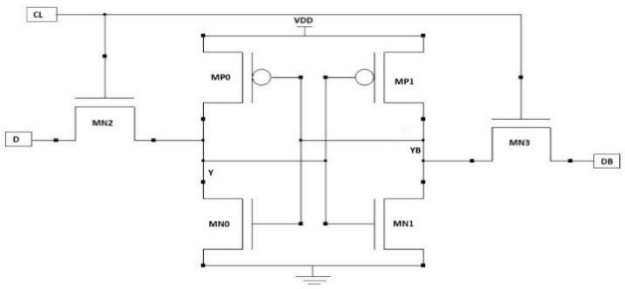

(c)

Fig -2 (a) Block diagram of multi-supply design application (b)multiplexer 2:1(c)SRAM cell

1) 2:1 Multiplexer: The figure-4 shows the multiplexer. In the circuit is implemented in a CMOS logic 2:1 multiplexer, transistors turn on due to a select signal, S and SB, its complementary value of S. While S = 0 (SB = 1), MP1, MP2, MN0, and MN1 turn ON allowing A1 to propagate into the output, S = 1 (SB = 0), MP0, MP3, MN2, and MN3 turn ON and allow the propagation of A2 into the output. Lastly, the MP4 and MN4 form a CMOS inverter that buffers out the output; therefore, one is assured that B has the required logic strength.

2) Voltage Level Shifter: As the SRAM'S cell required a voltage to store the data and operate efficiently at the 1.2V , mux output will store in the SRAM'S cell but the output voltage of the mux is 200MmV itself .To store the data we can increases the voltage level by voltage level shifter it converts the output of the mux 200mV into the 1.2V and given the input of the SRAM's cell at D and it's complementary input DB

3) Static Random Access Memory (SRAM): The given 6T Static-RAM cell is comprised of two cross-coupled inverters, MP0-MP1 and MN0-MN1, that store one bit of data and two access transistors, MN2-MN3, controlled by the control line CL for read and write operations. The data is complementary and carried out through the bit lines D and DB. The inverters keep Y and YB in opposite states during hold mode, with CL = 0. In a write operation, CL = 1, then D and DB determine the value stored at the cell, where D = 1, DB = 0 and stores '1' at Y and '0' at YB, and where D = 0, DB = 1 and stores '0' at Y and '1' at YB. By the WL =1 in the read operation it stores the data passed by the bit lines.

Every block of the application of multi supply design is implemented Individually in a 45nm technology in a cadence virtuoso and verified its outputs, and later on implemented in a multi-supply design and verified its outputs.

3. Simulation Results

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The efficiency and performance of the multi-supply design application and the proposed voltage level shifter was calculated by performing simulation of the design with a 45nm technology in cadence virtuoso.

And also implemented the different type of designs in voltage level shifters are already existed in same technology and compared the power, delay and power delay product and made analysis graph of different circuits at the different VDDL voltage changes as shown in below figure-9,10.

A. Waveforms of Proposed Design

Fig 5. This figure shows the output plots of the proposed voltage level shifter of input node X, output node Z. The designed proposed circuit is simulated for the input signal with risetime and fall-time of 2pS. The proposed design involves highest supply voltage of 1.2V, lowest supply voltage of 200mV and at a temperature of 25 °C. The proposed circuit attained a power consumption of 1.041nW@ 200mv and the propagation delay obtained of 17.77nS for a input supply signal of the 200mV.

Table II comparison of the proposed voltage level shifter and different type of the voltage level shifters in terms of the delay, power consumption and power delay product (PDP). The proposed circuit consumes 1.041 nW, which is lower than most designs except for [5] (0.079 nW), [9] (0.162 nW), and [8] (0.259 nW).

However, power alone does not determine the best design; delay and PDP must also be considered. The delay of the proposed circuit is 17.77 ns, which is much lower compared to most of the designs. For example, [5] has very poor power 0.079 nW, which suffers with quite high delay value of 435 ns. Similarly, [8] has a delay of 561 ns, which is much slower. PDP is the most critical metric for comparison as it considers both power and delay. The proposed circuit has a PDP of 0.018 fJ, which is the second-best among all designs, only slightly higher than [3] (0.016 fJ), but in terms of power it will be high so we also prefer proposed circuit then [3]. Most other designs have significantly higher PDP values, such as [4] (78.5 fJ), [7] (0.111 fJ), and [8] (0.145 fJ).

B. Multi supply design application waveforms

Figures 6 and 7 show simulated waveforms for the multiplexer 2:1and Static-RAM cell, respectively. In Figure 6, A1 and A2 are set to 200mV, and the whole design is supplied at 200mV. Therefore, the B value obtained was 200mV also. Thus, the multiplexer output is verified.

The operation details of an SRAM cell are shown in Figure 7. Provide a bit line voltage of 1.2V to bit lines D and DB while providing a supply of 1.2V to CL. When power is applied

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through the SRAM cell at the level of 1.2 V, data on bit line D finds storage at the output Y where data on the other bit line DB find storage at output YB at 1.2 V also. This serves as a form of validation with regard to SRAM cell functioning in accordance to its expected supply conditions.

Figure 8 It will represent the output waveform of multi-supply design application. Here, it also shows signals that include an input of multiplexer (A1 and A2), select line (S), multiplexer output (B), output of the voltage level shifter (Z), and SRAM signals (CL, Y, and YB). The design functions at various supply voltages. The multiplexer will operate at voltage of 200mV. The voltage level shifter functions at two supply voltages of 200mV and 1.2 V. The Static-RAM cell works at 1.2V.

From the simulation results in Figure 8, the multiplexer output B, which is originally 200mV, is successfully converted up to 1.2 V by the voltage level shifter at the Out-put node Z. This Out signal is then supplied as an input to the SRAM cell at D, while DB carries its inverted form. When CL is low, the previously stored data remains unchanged at Y and YB. In that case, out is 1.2V and that is correctly written into Y; its complement, however, in DB will be written to YB.

In this simulation, we can observe that the proposed level shifter is suitable for the multi-supply design has efficiently converted the 200mV output of the 2:1 multiplexer to 1.2 V by using voltage level shifter, and successfully stores it in the SRAM cell, thereby establishing the efficiency of the voltage level shifter as well as the overall functionality of the system

Table-II: Comparisonof the different type of voltage level shifters

	Power(nW)	Delay(ns)	PDP (fJ)
Proposed circuit	1.041	17.77	0.018
[4]	262	299	78.5
[5]	0.079	435	0.034
[7]	1.05	106	0.111
[8]	0.259	561	0.145
[9]	0.162	216	0.035
[11]	1.46	35.7	0.052

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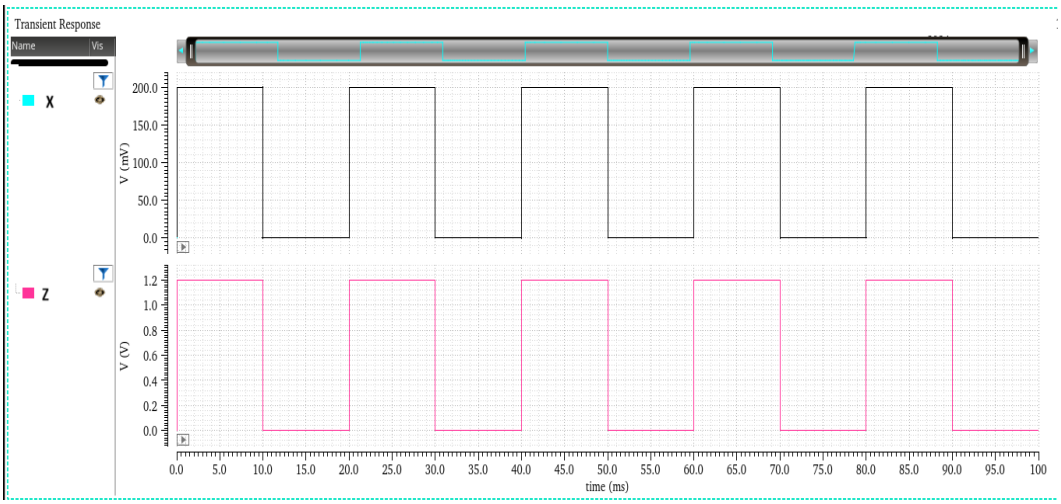
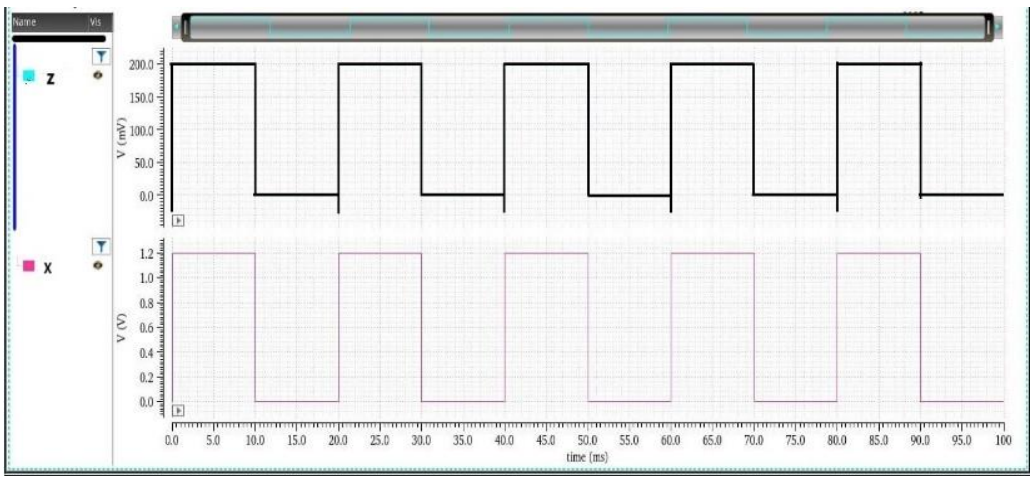
[18]	0.48	262	0.125
[3]	0.222	72.32	0.016



(a)



(b)

Fig 3: (a)Transient Output waveform of voltage level shifter from low to high(b) Transient Output waveform of voltage level shifter from high to low

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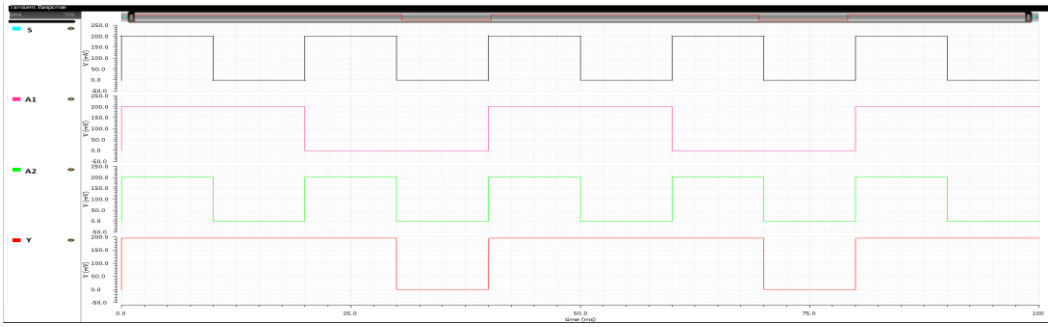

Fig 4: Multiplexer Output waveform

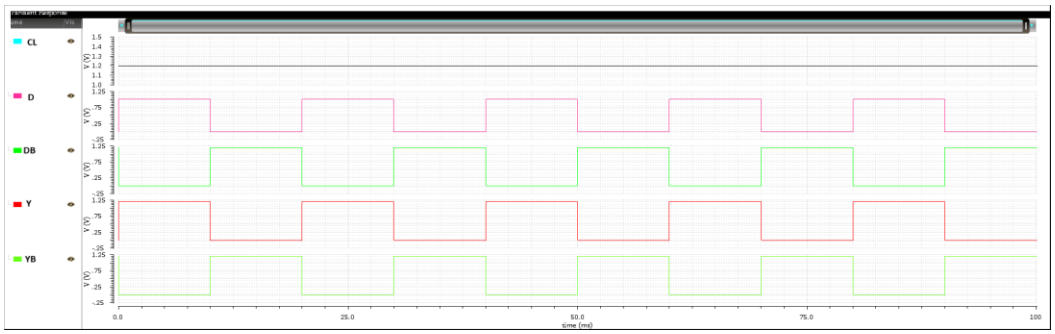

Fig 5: Output waveform of the SRAM cell

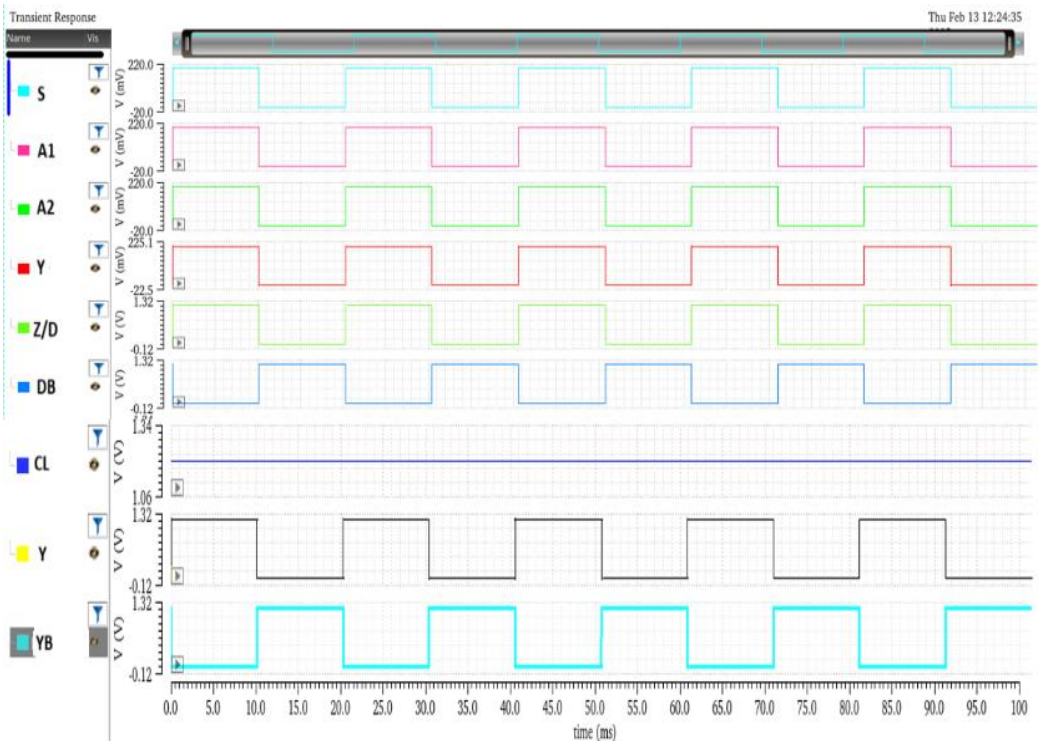

Fig 6: Output waveform of multi-supply design application

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The voltage level shifter (VLS) that proposed in this paper has a better performance in multi-supply design application as compared with some already existed [5][7]. The comparison of the application is shown in table III. By that the proposed design is suitable for the low voltage digital circuits as compared with some existing method.

Table-III: Comparison of the multi- supply design applications

	Power(µW)	Delay(µS)	PDP (nJ)
Proposed circuit	6.12	137.4	0.841
[5]	11.82	256	3.025
[7]	10.61	288.5	3.06

As compare with application the proposed circuit consumes a low power 6.12 µW than [5],[7].and also very fast operation and produces a less delay with respect to [5],[7]. And also, a one of important factor PDP will also less as compares with the [5],[7]. The performs is very well in terms of power, propagation delay and power delay product (PDP) of the proposed circuit.

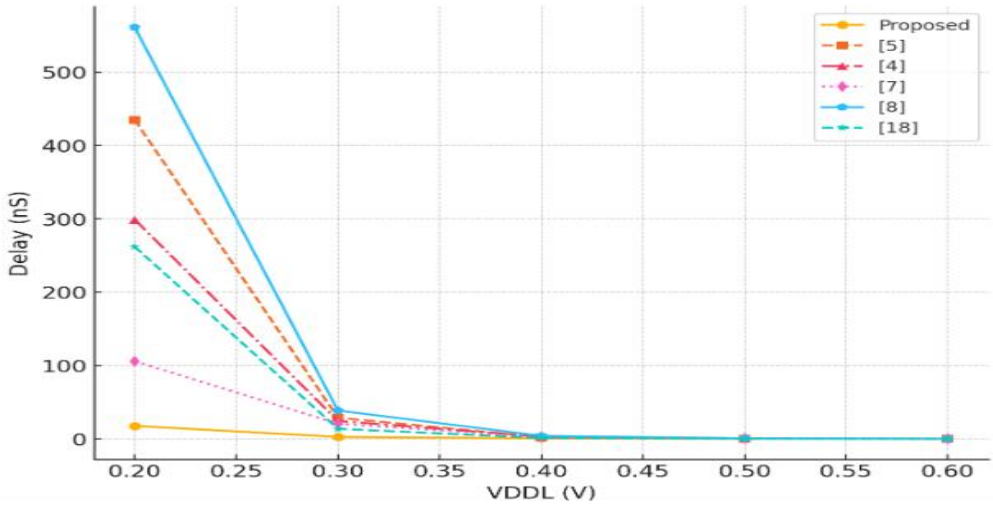

Fig 7: Delay analysis of the proposed VLS versus existing designs at different VDDL

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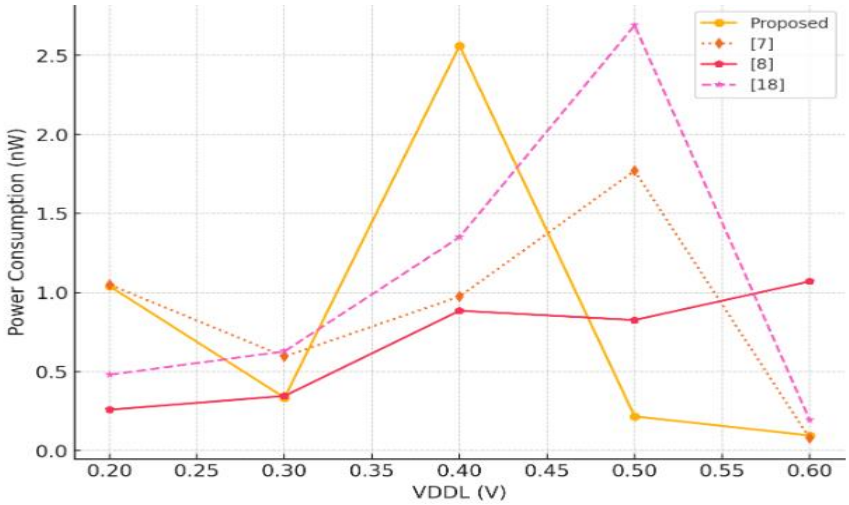

Fig 8: Power analysis of the proposed VLS versus existing designs under different VDDL conditions

4. Conclusion

The paper presents of proposed voltage level shifter with uses of novel current mirror technique and also by using hysteresis transistors by that reduces some drawbacks that already have in existed circuits like, voltage swing, idle power consumption. The proposed voltage level shifter achieves a very rapid conversion and proposed design will suitable for the multi-supply voltage applications, and also for low power applications. As the measurement results of the proposed voltage level shifter has less delay a 17.7 ns at 200mV. The proposed voltage level shifter achieves 200mV to 1.2V wide range voltage conversion.

REFERENCES

[1] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012, Doi: 10.1109/TCSI.2011.2177004.

[2] J. Lee et al., "A self-tuning IoT processor using leakage-ratio measurement for energy-optimal operation," IEEE J. Solid-State Circuits, vol. 55, no. 1, pp. 87–97, Jan. 2020, Doi: 10.1109/JSSC.2019.2939890.

[3] S. Lütkemeier and U. Rückert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[4] V. L. Le and T. T. Kim, "An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output buffer in 65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 5, pp. 607–611, May 2018.

[5] S. Kabirpour and M. Jalali, "A power-delay and area efficient volt age level shifter based on a reflected-output Wilson current mirror level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 2, pp. 250–254, Feb. 2020, Doi: 10.1109/TCSII.2019.2914036.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

[6] H. You, J. Yuan, W. Tang, S. Qiao, and Y. Hei, "An energy-efficient level shifter for ultralow-voltage digital LSIs," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 3357–3361, Dec.2020, Doi: 10.1109/TCSII.2020.2980681.

[7] L. Fassio et al., "A robust, high-speed and energy-efficient ultralow voltage level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 4, pp. 1393–1397, Apr. 2021, Doi: 10.1109/TCSII.2020.3033253.

[8] K. Kim, J. Y. Kim, B. M. Moon, and S.-O. Jung, "A 6.9-µm2 23.26-ns 31.25-fJ robust level shifter with wide voltage and frequency ranges," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 4, pp. 1433–1437, Apr. 2021.

[9] M. N. Sharafi, H. Rashidian, and N. Shiri, "A 38.5-fJ 14.4-ns robust and efficient subthreshold-to-suprathreshold voltage-level shifter comprising logic mismatch-activated current control circuit," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 70, no. 6, pp. 1906–1910, Jun. 2023, Doi: 10.1109/TCSII.2023.3237083.

[10] H. Jeong, T.-H. Kim, C. N. Park, H. Kim, T. Song, and S.-O. Jung, "A wide-range static current-free current mirror-based LS with logic error detection for near-threshold operation," IEEE J. Solid-State Circuits, vol. 56, no. 2, pp. 554–565, Feb. 2021, Doi: 10.1109/JSSC.2020.3014954.

[11] E. Låte, T. Ytterdal, and S. Aunet, "An energy efficient level shifter capable of logic conversion from sub-15 mV to 1.2 V," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 11, pp. 2687–2691, Nov. 2020.

[12] J. Park and H. Jeong, "Energy-efficient wide-range level shifter with a logic error detection circuit," IEEE Trans. Very Large-Scale Integration. (VLSI) Syst., vol. 31, no. 5, pp. 701–705, May 2023, Doi: 10.1109/TVLSI.2023.3244569.