Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

Domino Logic Low Leakage Clock Keeper (LLCKDL) for Effective CMOS Logic Gates

Dr.M. Chennakesavalu[1], B.Chandra obulreddy[2], U. Tanooja[3], B. Indra senani[4],S. Prudhvinath Reddy[5]

[1]Department of ECE
RajeevGandhiMemorialCollegeofEngineering&Technology,Nandyal,India,518501
[2,3,4,5]Department of ECE
RajeevGandhiMemorialCollegeofEngineering&Technology,Nandyal,India,518501
Corresponding author: chennakesavuluece@rgmcet.edu.in

Abstract:-

Propagation delay and power consumption are two critical challenges in deep-submicron CMOS VLSI semiconductor circuits. High leakage currents and increased noise sensitivity further exacerbate these issues, demanding innovative design techniques to enhance efficiency. This study presents a novel approach for designing CMOS logic gates using the Low Leakage Clock Keeper Domino Logic (LLCKDL). The proposed methodology aims to significantly reduce leakage power while improving noise immunity and operational efficiency. The LLCKDL technique incorporates an optimized clock-keeper circuit to minimize unnecessary power dissipation in dynamic logic while maintaining robust signal integrity. To validate its effectiveness, a 16-bit OR gate was designed and simulated using 45 nm CMOS GPDK technology in the Cadence environment. Comparative analysis with existing design methodologies demonstrates substantial improvements. Specifically, LLCKDL achieves an 86.36% reduction in average power consumption, a 56.93% decrease in propagation delay, and an 86.90% improvement in the energy-delay product (EDP). These results highlight the efficiency of LLCKDL in reducing power dissipation while ensuring high-speed operation, making it a promising design paradigm for next-generation low-power CMOS circuits. The proposed approach is particularly beneficial for high-performance VLSI applications, where both power efficiency and speed are crucial. By mitigating leakage power and enhancing noise resilience, LLCKDL offers a viable solution for improving the performance of deep-submicron CMOS logic circuits, paving the way for more energy-efficient and reliable semiconductor devices.

Keywords: — Power consumption, Delay, Domino logic, GPDK 45nm CMOS

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

1. Introduction

Because they utilize less power and switch more quickly than static logic circuits, dynamic logic circuits are frequently used in memory design and high-speed signal processing applications. But because of their low threshold voltage, they frequently become troublesome and are negatively impacted by noise interference. The supply voltage is reduced to increase energy efficiency as technology develops. An effective dynamic logic circuit would require a low threshold voltage and subsequent management of leakage and dynamic power consumption [1,2].

The circuit capacitance's charging and discharging processes consume an excessive amount of dynamic power, and the circuit short-circuits to ground, wasting short-circuit power. And practically, whenever a transistor turns off, there will be some leakage power due to the leakage currents. To address these power losses and improve noise immunity, modern circuit designs focus on reducing supply voltage and device sizes. However, if the device dimensions are shrunk, the length of its channel will be reduced and the short-channel effects will also be reduced [3,4].

The research describes LLCKDL, a cutting-edge method for improving CMOS logic gates. This strategy aims to lower leaky power consumption and enhance noise performance. Using Cadence's GPDK 45 nm CMOS technology, an OR gate with 16 inputs has been constructed and simulated at a clock frequency of 10 MHz. The performance results were analysed using power consumption, UNG, and propagation delay. The results show that the proposed design reduces power consumption by at least 74.19%, improves delay by 14.91%, and surpasses the previous designs in terms of energy delay product (EDP) by 67.39%.

In the second subsection of this study, the existing domino logic models were reviewed, and in the third subsection, the suggested CMOS 45 nm logic architecture was described. With this technique, enhanced noise immunity and reduced leakage power are obtained by stacking transistors in an efficient manner to realize high-speed gates with large fan-in" Low propagation latency and power consumption are ensured here by resolving the conflict between the evaluation network and the keeper transistor. This circuit is considerably superior to earlier designs.

The noise immunity of dynamic circuits is negatively impacted by additional supply voltage reduction. Next, technological scaling is allowing the reduction of threshold voltage so that thus enhancing the leakage increases the thinning of gate oxide. The above leakage might improve noise and leakage problems leading to the discharge of the precharge node in domino logic circuits at high frequencies. The presence of multiple parallel paths in the

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

evaluation logic contributes to higher leakage currents, especially in large fan-in gates, leading to undesirable discharge of the precharge terminal and degraded noise resistance.

To counter this situation, a bigger keeper transistor is advantageous for noise immunity. Higher power dissipation and delay in propagation are drawbacks, though. A larger keeper transistor could lead to conflict between the evaluation logic and the keeper transistor itself by slowing down circuit functioning. At the expense of higher energy consumption, a big keeper transistor will also improve noise immunity and lower leakage current.

Ultimately, the three primary power components that regulate logic circuit power are switching power, short-circuit power, and power leakage. The proposed LLCKDL method effectively addresses these issues by enhancing transistor design, reducing leakage currents, and boosting noise performance, making it a promising strategy for future high-speed digital circuits.

2. Existing Techniques in Domino Logic: A critical Review

Domino logic circuits are favoured over other dynamic logic-based digital circuits because of their low power and chip area usage. Large-scale memory systems and fast CPUs are their primary uses. Domino logic utilizes a single PMOS in the pull-up network (PUN), whereas dynamic logic uses many PMOS depending on the number of inputs. One of the primary distinctions is this. This design difference results in higher area and power efficiency for Domino logic circuits.

However, domino logic designs are significantly affected by gate leakage, including subthreshold leakage, which poses a major challenge. Additionally, improper scaling of components can lead to reduced noise immunity in these circuits. Researchers have explored various methods to mitigate leakage power and improve noise resistance in domino logic [11].

In order to improve CMOS domino logic operation, Garg and his colleagues proposed a sharper interference in comparison to low voltage noise contingent domino logic (LVNIDL). The technique was then extended to wide fan-in OR gates and validated using 32nm CMOS HSPICE simulations. For transient analysis, the proposed model operates at a voltage of 0.9 V DC power and a clock frequency of 100 MHz. According to the work's findings, the design is faster and more energy-efficient than any other currently used technique, with a maximum latency improvement of 56.25% and a 76.07% decrease in power savings over CPVT [12].

An ONOFIC pull-down approach was proposed by Magraiya [13] and associates to reduce subthreshold leakage in 32 nm domino circuits based on FinFETs. Both dynamic and inverted pull-down networks incorporate ONOFIC components into their architecture. In comparison to LECTOR-based domino circuits, an OR16 circuit employing this method reduced subthreshold leakage by 48.1% in the low-power (LP) configuration and by 74% in the short-gate (SG) setup, according to HSPICE simulations conducted within a 32 nm BISM4 framework.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

Tiwari et al. [14] presented a novel circuit design known as NSCDH, which facilitates the construction of OR gates ranging from 8 to 128 inputs while allowing cascading to subsequent stages. The design integrates an intermediate isolation mechanism that maintains current-free node states, optimizing circuit efficiency. Compared to CDDK, this approach demonstrated a 44.6% reduction in power consumption and a 16.1% improvement in noise immunity for 8-input gates, while achieving a 24.4% reduction in power usage at 128 inputs. HSPICE was utilized to conduct circuit modelling along with conventional 90 nm PTM transistor models.

3. Implementation of different Domino Logic

Figure1showstheFLDL [15]circuitinitsinitialimplementation.Thevariationofcharge storedinthe outputcapacitanceasa resultofjunctioncapacitance(Cj) [16]isasignificantdrawbackofthisdesign.The keeper, which complements the precharge transistors, isintroducedtoovercomethisdifficulty.Further,keeper transistor is one that is driven from the output of the circuit beyond whichit acts to enhance circuit stability In other words, the keeperprevents the unintended release of dynamic nodes through PDNleakage and the related charge-sharing.

IssuesSimplystated,theprimarylimitationofFLDListhePDN'sleaky properties during evaluation, which takes placeindependent of the magnitude of the applied voltage across allevaluation logic inputs. A considerable contention current flowsvia the keeper and the PDN when the keeper transistor's size isincreasedproportionatelytothe PMOS-PDNcurrent, raisingthecircuitdelay.

Numerically,

$$Kr=W_{kp}/W_{ev}$$

Where W_{kp}= TransistorWidthoftheKeeperCircuit
W_{ev} = width of the evaluation logic circuit

To switch off the power supply during the evaluation phase, anadditional transistor (named N1) was placed between theevaluation logic and ground. FDL [19] is the name of the enhancedcircuit shownin Figure2.Byincreasingdelay,the foot transistor(N1) raises the circuit's overall latency.Additionally, as thenumberofinputs(fan-in)rises, the circuit’s noiseimmunitytendsto worsen.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

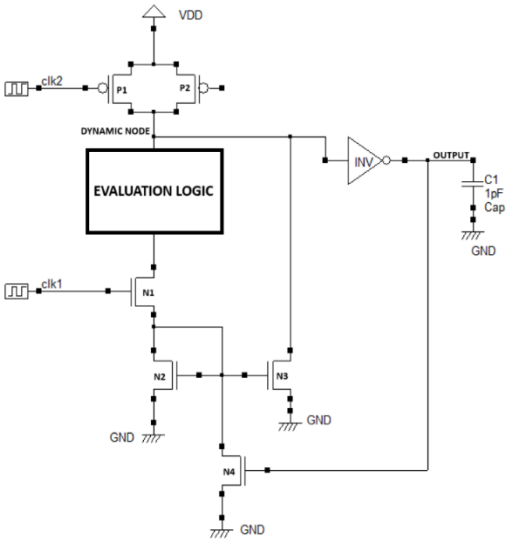


Fig.1.FLDLCircuitArchitecture [15]

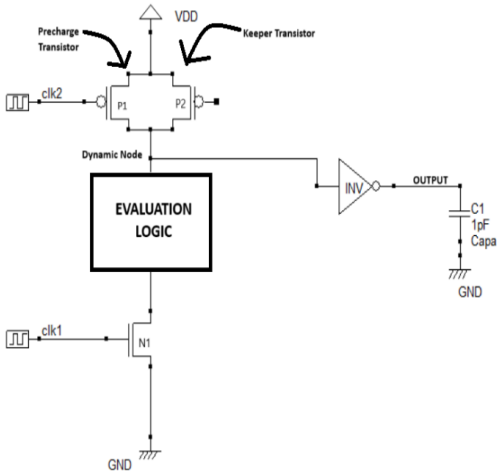


Fig.2.FDLCircuitArchitecture[19]

Figure 3 illustrates another domino logic circuit that creates astacking effect by using an extra transistor (N2). Despiteimprovingnoiseimmunity,thismodificationcausesanadditionaldelay in the evaluation process. To lessen this delay, a currentmirror circuit hasbeen constructed using transistors N2 and N3.This technique, which is known as CMFD, boosts speed at thecost of increased sizeand power consumption due to theadditional transistors N2, N3, and N4.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

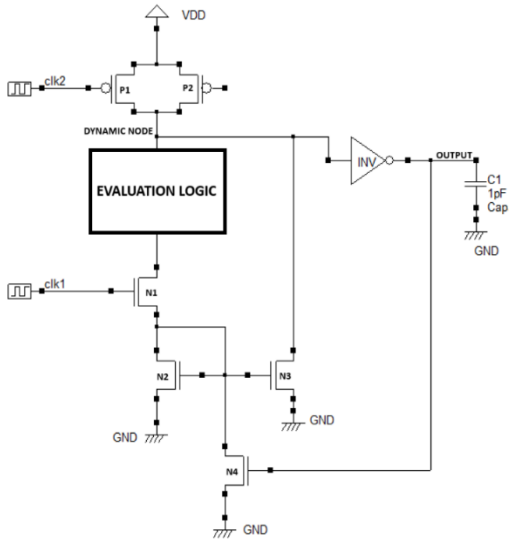


Fig.3.CMFDL CircuitArchitecture

Figure 4 illustrates an additional technique that uses an NMOStransistor(M0)inconjunctionwithANDgatestofurtherimprovecircuit efficiency.One major drawback of this approach is theadditionofafloatinggatetotransistorMN2,whichraisespowerconsumptionduringtheprecharg ephase.Thisapproachisknownas(M-HSCD).

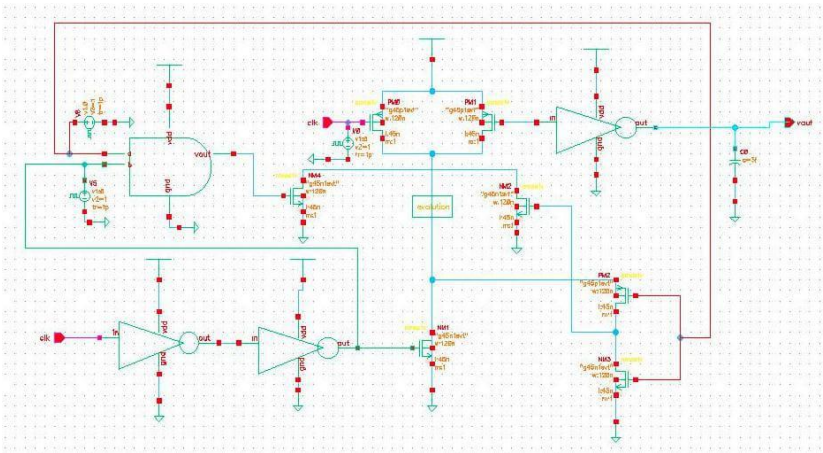
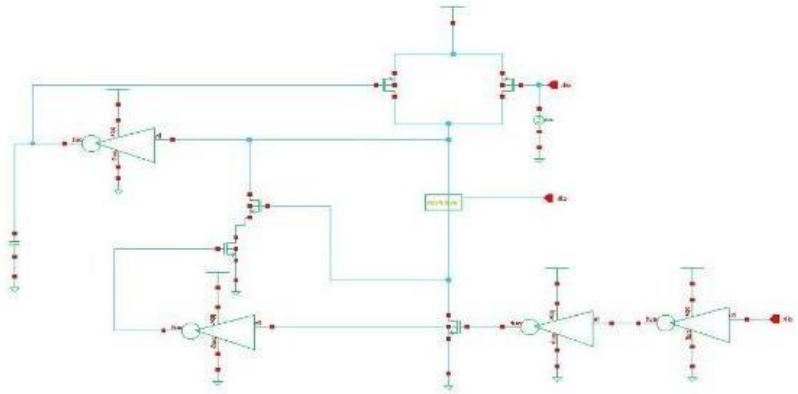


Fig.4.M-HSCDCircuitArchitecture[18]

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

An alternate domino arrangement is shown in Figure 5, wheretransistors N2 and N3 are stacked between the ground and thedynamicnode.Thesetransistorsworktogetherwithtransistor N1to enable controlled switching. The floating gate problem in M-HSCD is effectively resolved by this method,



called CEDL,which increases power efficiency.

Fig.5. CEDLCircuitArchitecture [18]

AnalternatedominoarrangementisshowninFigure5,wheretransistorsN2andN3arestackedbetweenthegroundandthedynamicnode.Thesetransistorsworktogetherwithtransistor N1 to enable controlled switching.

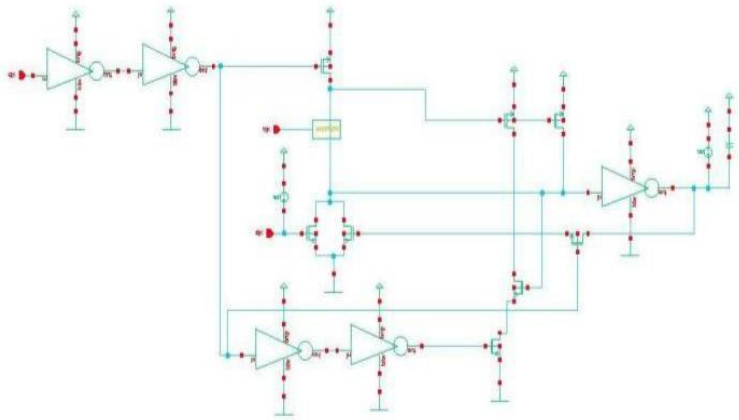


Fig.6.CSK-DLCircuitArchitecture[18]

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

4. Novel high performance Domino Logic

The preceding section dealt with options for actualizing domino logic circuits. Here, we describe a new design that is intended to further improve the capabilities of domino logic. The suggested design, illustrated in Fig 7, is referred to as LLCKDL.

Thiscircuitconsistsofafooter-equippedNMOStransistor(N1),a clocking PMOS transistor (P1), a pull-down networkconstructed entirely of NMOS transistors,and akeeper made upof two PMOS transistors (P2 and P3) connected in series. Instandbymode,thecircuitstateismaintainedandtheclocksignalis managed by a MUX. One of the MUX's inputs receives theclock signal, while the other receives the circuit's output signal.

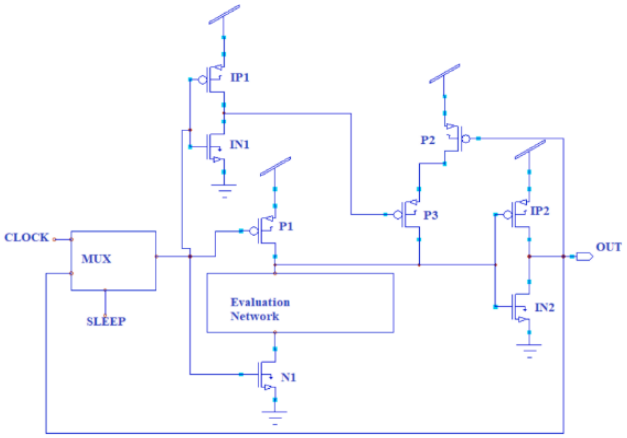


Fig.7.SuggestedLLCKDL.

Whenthesleepsignalissetto"0"theMUX'soutput(y)canstayin activeoperation by following the clock input. When the sleepsignal in standby mode is set to "1" the MUX output uses thecircuit's output signal (out) as its value. This circuit operates in two modes: Active and Standby.

:The sleep signal is turned off but still functional when the clockisinactivemode.TransistorP1isactivatedtochargethedominonode during the precharge phase when the clock signal is "0".Both P3 transistor and keeper are temporarily deactivated during the Eval stage to avoid conflict. If the pull-down network is active, transistor N1 disconnects the dynamic node when the clock signal changes to "1". Transistor P2 stays off if the output is "1" guaranteeing that the keeper stays idle. If the output changes to "0" and the pull-down network stops conducting, the P2 transistor activates.Since the clock remains "1" transistor P3 also activates, maintaining the dynamic node at "1" through thekeepercircuit.

STANDBY:The output value determines how the circuit behaves in standbymode. When transistor P2's output (out) is set to "1" the keeperstays idle. When transistor N1 activates, the pull-down networkconductsandthedominonodeisdraggedtoground,ensuringthatthe output remains at "1".When transistor P3's output (out) is set to "0" the keeper isdeactivated.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

Transistor P1 pushes the domino node to a highvoltagelevelinthisscenarioevenwhenthepull-downnetworkisnot conducting, maintaining the output at "0".

The suggested architecture improves upon conventional dominologic by adding an extra PMOS transistor (P3) in the keepercircuit.Thereasoninghereisthattheactivationboosterkeepsthecontrollerinertinthesupervisionofunderstandingduringthefirstphase of application, inhibiting content by keeping powerrequirements within manageable limits. 2 to 1 MUX and 2 input OR gate are designed using this method in this paper.

MUX Design:Figure 8 depicts a 2-to-1 MUX (MUX) using Gate DiffusionInput (GDI) logic. The PM0 and NM0 transistors make up theMUX.Achievingfull-swingoutputvoltageisafrequentproblemwithGDI-basedmultipliers.TransistorNM2isputacrossPM0toresolvethisproblemand preservecomplete voltageswing.Fig9shows the simulation results for the suggested MUX.

TheMUXoperatesasfollows:

Upon receiving a high selection signal (S), input B is sent tooutput.Uponalowselectionsignal(S),inputAissenttooutput.

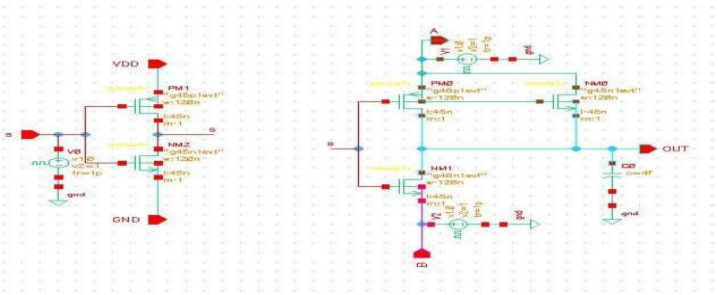


Fig.8. 2to1MUX

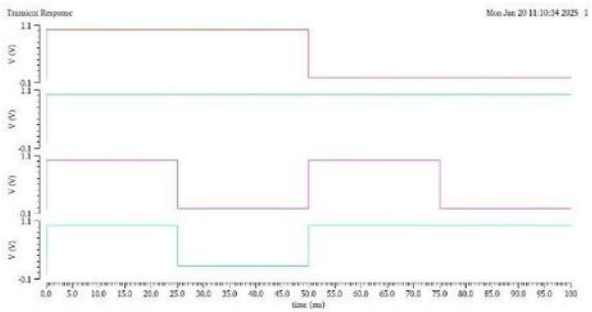


Fig.9. 2to1MUXtransient simulation.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

Input OR gate: Figure 10 illustrates how the LLCKDL technique is used tocreate a 2-input OR gate. The N4 and N5 NMOS transistors areconnected in seriesby this OR gate forlogical evaluation. In theprecharge mode, the output voltage stays at its maximum whenthe sleep signal is set to "0," In active mode, the clock signal isconnected to the MUX output (y), and the sleep signal is "0."

Theoutputremainsatzerowhenthesleepsignalinstandbymodeissetto"1."TheORgate'sinputsaredenotedbyAandB,andthedynamicnodevoltageisrepresentedbyX.Whentheclocksignalis weak, the precharge transistor charges the dynamic node.Consequently, theinverter causes theoutput voltage to drop andthedynamicnodevoltagetorise.Thevaluesenterednowhavenoeffecton the output.The assessment phase starts when the clocksignal is high. The dynamic node discharges if one of the inputs(Aor B) is high.After a small delay caused by the inverter, thisdischargeforcestheoutputtotransitiontohigh.Figure11showsthematchingwaveformsforthevariousinputconditionsofthe2-input OR gate.

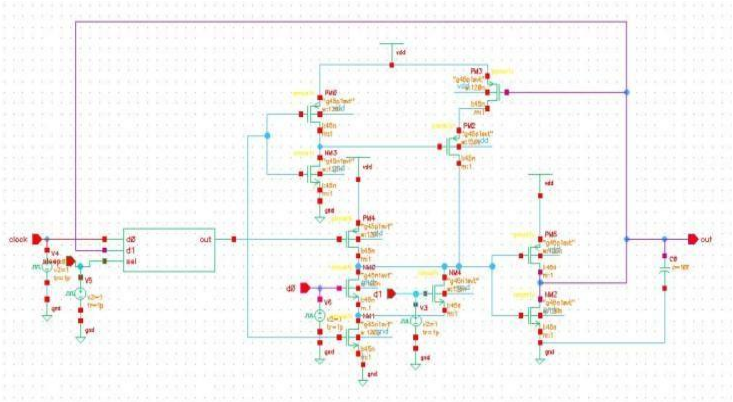


Fig.10.Atwo-input ORgateusingthesuggested Dominologic

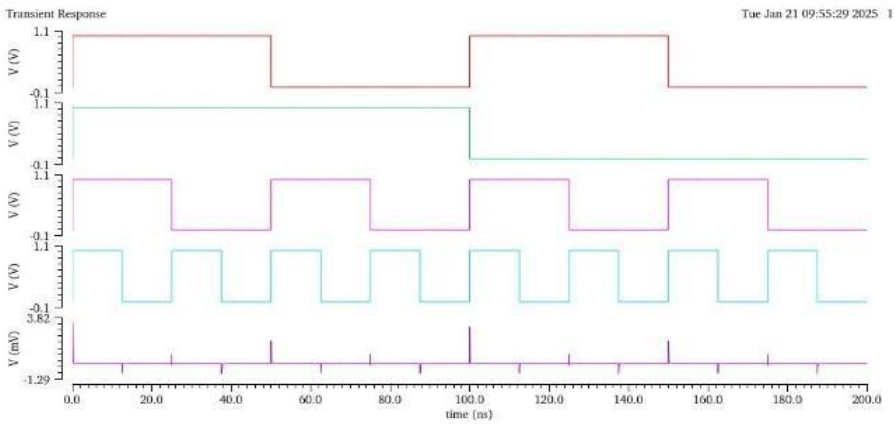


Fig.11.SimulatedWaveformofSuggestedTwo-InputORGate

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

5. Implementation and Evaluation of the suggested Domino logic design

Numerous domino logic techniques, such as CEDL, CMFD,CSK-DL, HSCD, FDSTDL, and GPKD, are discussed andusedin this work along with a recently proposed technique in theCMOS domain. To compare the performance of these designs,simulations are performed using the Cadence Spectre toolconsidering the 45 nm technology node. Transistor N1's widthwas increased to fourtimes the minimumchannel length (L_{min})in the new design to reduce circuit delay. whereas conventionaldesigns use only twice L_{min}. Here, L_{min} is defined as theminimum channel length, which is equal to 45 nanometre. ThewidthoftheparallelNMOStransistorwassettodoublethevalueof L_{min} in the evaluation block. Furthermore, the width ratioPMOS to NMOS in inverter was kept constant at 2.5 (W_p/W_n),with PMOS and NMOS dimensions set to 4Lmin and 2Lmin,respectively. The keeper transistor (P2) was defined as $4L_{min}$while the precharge transistor (P1) was set to $2L_{min}$.

Comparison of Various Domino Logic Techniques:

CMFD(CurrentMirrorFeedback Domino Logic): Byusingthestackingeffect,anadditionalN1transistorlowersleakage power. N4 is included to minimise noise, and currentmirror transistors (N2 & N3) are included to decrease latency.

CEDL: connects the dynamic node using a pair of stacked NMOStransistors(N2&N3),affectingvoltagelevelsaccordingtothesizes of N1 and the evaluation transistors.

GPKDL: Implements a grounded PMOS keeper circuit toenhance noiseimmunity and stability.

FDSTDL (FULLY DEPLETED SUBTHRESHOLDDOMINOLOGIC): Makes use of NMOS stacking (N2 & N3) to improve powerefficiencyandlowerleakagecurrent.usesatinyPMOSkeepertokeep the circuit stable and avoid excessive power loss. APMOSkeeperisnecessaryforeachofthesecircuitsinordertoguarantee correct domino logic operation. However, a largerPMOS keeper is required as the number of domino logic inputsrises. Higher contention currents between the NMOS pull-downnetwork and the PMOS keeper result from this, which lowerscircuit efficiency and raises dynamic power consumption.

SuggestedApproach: To solve these issues, a new domino logic technique using adelayedkeepercircuitwithclockgatingwasdeveloped.In the M-HSCD arrangement with FDL circuits, transistors N2,N3, and P3 are utilized to fix the foot node (N) voltage andminimize current leakage during the evaluation phase. There weretwo inverters that delayed the clock

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

signal that controlledtransistorN1.NMOStransistors(M0)andanANDgate(G)wereintegrated to improve evaluation efficiency.

CSK-DL(Clock-SkewedKeeper Domino Logic): In the FDLarrangement, the N2, N3, N4, P2, and P3 transistorswork together. Transistors N2 and N3 guarantee appropriatedynamicnodedischargingduring theevaluationcycle,whilethekeeper circuit is shut off prior to the evaluation phase, reducingcontention current. Although this design eliminates the conflictbetween NMOS pull-down networks and PMOS keepers, theadditional gates increase the layout area and power dissipation.

OptimizationsinSuggestedDesign: Newly suggested domino logic circuitry stacks transistors toreduceleakageenergy consumption at thesame timeasincreasenoise immunity. The following important elements would bebrought about by the architecture in order to ultimately limitpower and delay conflict between the keeper and the evaluationnetwork. Duringthe evaluationphase, PMOS(P3)introducedtoakeepercircuitisfirstswitchedoff.Thisfurtherminimizespowerdissipation and gets rid of contention current. A linked clockgating MUX is part of the updated keeper circuit, which allowsfor exact clock signal management. The MUX helps maintaincircuit state in standby by selecting either the clock or outputsignal (out).

KeyMetricsforPerformanceAnalysis:

To assess thenoise immunity,power efficiency, and robustnessofdifferent domino logic circuits, several key performanceparameters were considered

PropagationDelay (t_p):

This measures the amount of time it takes for a signal to getfromtheinputtotheoutput.evaluatedatthecircuit'sevaluationphase using the following formula:

$$t_p=(t_{pl}+t_{ph})/2 \quad (6)$$

Theriseandfalltimedelaysaredenotedbytheletterstplandtph,respectively.

AveragePowerConsumption (P_{avg}):

Determined through transient analysis over 500 ns. A 10 MHzclock frequency and a 1.2Vpulse applied to each input are usedforsimulations.

ProductofPowerDelay (PDP):

Calculatestheoverallenergyusedforswitchingoperations:

$$PDP=AveragePower\times Delay \quad (7)$$

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

EnergyDelayProduct(EDP):

Evaluatesthecircuit'senergyefficiencywhilecarryingoutlogicoperations:

8. EDP=PDP × PropagationDelay

UnityNoiseGain(UNG): Determinesthecircuit'snoiseimmunitybyapplyingashorthigh-amplitude pulse to both inputs of the evaluation circuit.

TABLE 1: Performance comparison table of existing and proposed techniques to realize 16 input OR gate

Topology	Delay (ps)	Average Power Consumed (μW)	Power Delay Product (PDP) (10^{-18}) (Ws)	Energy Delay Product (10^{-18}) (EDP) J^2
CEDL	64.48	1.02	65.7696	4.24
CMFDL	86.24	1.42	119.6208	10.316
CSK-DL	53.37	1.76	93.9312	5.013
HSCD	47.76	1.34	63.9984	3.056
GPDK	43.64	0.93	40.5852	1.771
LLCKDL (Proposed)	37.14	0.24	8.9136	3.31

6. Conclusion

In order todesign a 16-bit OR gate, the novel structure was integrated withcontemporary domino logic techniques. There are notableimprovements in power efficiency, delay, power-delay product,andenergy-delayproduct as compared toconventional techniques. This realization is well suitable for low-powerand high-performance applications.

Performance measures indicated that the suggested design reducespowerconsumptionby 76.47%,83.10%,86.36%,82.09%,and74.19% compared to CEDL, CMFDL, CSK-DL, HSCD, andGPDK, respectively. The Delay is also minimized by42.39%, 56.94%,30.39%, 22.24%,and 14.91% relative to thesame techniques. Furthermore, PDP is improved by 86.45%,92.55%,90.51%,86.08%,and78.03%,whileEDPsees enhancementsof78.10%,83.91%,85.23%,79.64%,and 67.39%,respectively.

Future research could explore on-chip training circuits andalternative low-power strategies to further optimize energyefficiency.Furtherresearchmayimproveoverallperformancebyfine-tuning keepertopology and optimising transistor aspectratios inpull-down network.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

REFERENCES

[1] S.H. Choi, B.C. Paul, K. Roy, Dynamic noise analysis with capacitive and inductive coupling, in: Proceedings of the 7th Asia and South Pacific Design Automation Conference(ASPDAC), 2002. January 11.

[2] T.K. Gupta, A.K. Pandey, O.P. Meena, Analysis and design of lector-based dual-Vt domino logic with reduced leakage current, Circuit World 43 (3) (2017) 97 104, https://doi.org/10.1108/CW- 03-2017-0013.

[3] I.C. Wey, C.W. Chang, Y.C. Liao, H.J. Chou, Noise-tolerant dynamic CMOS circuits design by using true single-phase clock latching technique, Int. J. Circuit Theor. Appl. 43 (7) (2015) 854– 865, https://doi.org/10.1002/cta.1976.

[4] A. Peiravi, M. Asyaei, Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, Integration 45 (1) (2012) 22–32, https://doi.org/ 10.1016/j.vlsi.2011.07.002.

[5] S.M. Sharroush, Y.S. Abdalla, A.A. Dessouki, Impact of technology scaling on the performance of domino CMOS logic, in: Proceedings of the International Conference on Electronic Design, 2008, pp. 1–3.

[6] S. Singhal, A. Mehra, U. Tripathi, Power reduction in domino logic using clock gating in 16 nm CMOS technology, in: Proceedings of the 6th International Conference on Signal Processing and Integrated Networks (SPIN) 2019, IEEE Publications, 2019, pp. 274–277.

[7] Y. Sun, W. He, Z. Mao, V. Kursun, Variable strength keeper for high-speed and lowleakage carbon nanotube domino logic, Microelectron. J. 62 (2017) 12 20, https:// doi.org/10.1016/j.mejo.2017.01.010.

[8] A.A. Angeline, V.S. Kanchana Bhaaskaran, Design impacts of delay invariant highspeed clock delayed dual keeper domino circuit, IET Circuits Devices Syst. 13 (8) (2019) https://doi.org/10.1049/iet-cds.2018.5410.

[9] M.R. Nandini, P. Mor, J. Keller, A comparative study of static and dynamic CMOS logic, Int. J. Curr. Eng. Technol. 6 (2016) 1019–1021.

[10] S. Garg, T.K. Gupta, Low power domino logic circuits in deep submicron technology using cmos, Eng. Sci. Technol. Int. J. 21 (4) (2018) 625–638.

[11] N. Liao, X. Cui, K. Liao, K. Ma, D. Wu, W. Wei, R. Li, D.Yu, Low power adiabatic logic based on finFETs, Sci. China Inf. Sci. 57 (2) (2014) 1–13.

[12] S. Garg, T.K. Gupta, A.K. Pandey, D. Pandey, P. Rajpoot, The effect of noise robustness on domino using silicon nano materials, Silicon (2024) 1–15, https:// doi.org/10.1007/s12633- 024-02854-8.

[13] J. Rajesh, Pandey, A. Kori, S. Magraiya, V. Gupta, T. Verma, Evaluation of dualONOFIC method for subthreshold leakage Reduction in domino circuit, Int. J. Electron. (2023), https://doi.org/10.1080/00207217.2023.2278439.

Power System Technology
ISSN:1000-3673

Received: 16-01-2025 Revised: 05-02-2025 Accepted: 12-03-2025

[14] M. Tiwari, V. Chaurasia, Nodal state comparison-based dynamic hold technique for low power OR gates in domino logic, IETE J. Res. (2023) 1–11, 10.1080/03772063.2023.2194263. https://doi.org/

[15] H. Mahmoodi-Meimand, K. Roy, Diode footed domino: a leakage tolerant high fanin dynamic circuit design style, IEEE Trans. Circuits Syst. I 51 (3)(2004)https://doi.org/10.1109/TCSI.2004.823665. 495–503,

[16] C.H. Cheng, S.C. Chang, J.S. Wang, W.B. Jone, Charge sharing fault detection for CMOS domino logic circuits, in: Proceedings of the International Symposium on Defect and Fault Tolerance in VLSI Systems, 1999, pp. 77–85, https://doi.org/ 10.1109/DFTVS.1999.802872.

[17] T.K. Gupta, K. Khare, Lector with footed diode inverter: a technique for leakage reduction in domino circuits, Circuits Syst. Signal Process. 32 (6)(2013)2707–2722, https://doi.org/10.1007/s00034-013-9615-2.

[18] S.A. Tawfik, V. Kursun, High-speed finFET domino logic circuits with independent gate-biased double-gate keepers providing dynamically adjusted immunity to noise, in: Proceedings of the of IEEE International Conference 2007, pp. on Microelectronics, 175–178, https://doi.org/10.1109/ICM.2007.4497687

[19] N. Gong, B. Guo, J. Lou, J. Wang, Analysis and optimization of leakage current characteristics in sub-65 Nm Dual Vt footed domino circuits, Microelectron. J. 39 (9) (2008) 1149–1155, https://doi.org/10.1016/j.mejo.2008.01.028.

[20] F. Moradi, T.V. Vu Cao, E.I. Vatajelu, A. Peiravi, H. Mahmoodi, D.T. Wisland, Domino logic designs for high performance and leakage tolerant applications, Integration 46 (3) (2013) 247–254, https://doi.org/10.1016/j.vlsi.2012.04.005