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Low Power and Energy Efficiency Techniques for Full Adder – Implementation, Comparison and Analysis in 45 Nm Technology

Dr. S. Govindarajulu[1], K. Sudheer[2], V. Eswar Manideep[3], E. Sharath Kumar[4], K. Kiran[5]

[1]Professor, Dept.of ECE, Rajeev Gandhi Memorial College of Engineering & Technology, Nandyal, A.P., India.

[2,3,4,5] Department of ECE, Rajeev Gandhi Memorial College of Engineering & Technology, Nandyal, A.P., India.

Corresponding Author: rajulusg09@gmail.com

Abstract: **-** The 1-bit full adder is a crucial digital component in arithmetic implementations, processors, and digital filters. Reducing its power consumption is essential for minimizing the overall power of digital systems. This paper presents an extensive study on various lowpower techniques for a 1-bit full adder, focusing on logic styles, hybrid digital styles, redundant components, and methods for reducing transistor count. Three techniques are explored: Gate-Diffused Input (GDI) for voltage swing reduction, redundant component-based multiplexers for power reduction and circuit simplicity, and hybrid module implementation combining different techniques. This work explores six proposed full adder (FA) designs: GDI1, GDI2, GDI3, GDI4, Mux based, Hybrid Full adders. The implementations are carried out using 45 nm process node using Cadence Virtuoso, with results analysed, tabulated, and compared. This study offers valuable insights into the effectiveness of different low-power techniques for 1-bit full adder design, enabling the development of energy-efficient digital systems. The 16T Hybrid FA design stands out as the most efficient in terms of power, delay, and Power Delay Product (PDP). MUX-based and GDI1, GDI2 implementations also show lowest power compared to traditional CMOS designs. Approximately 54.88% less power and 86.68% less delay is used by the Hybrid Full Adder than by the CMOS Full Adder.

Keywords: Full Adder, Energy,GDI, Hybrid Logic, Low Power, Mux based, Nanometer Technology, PDP

1. Introduction

A full adder is a fundamental building block in digital systems, used for arithmetic operations and digital signal processing. It affects performance and power metrics in circuits. As process

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nodes shrink, managing power density and heat becomes increasingly challenging, necessitating low power implementations.

The traditional CMOS full adder shown in Fig.1 consumes 28 transistors and are associated with high dynamic power dissipation. CMOS design is further classified into two subcategories: static and dynamic logic. Dynamic logic is area- and transistor efficient but suffers from charge sharing and recharge stage problems that are alleviated with high switching activity and large clock loads.

$$\text{Sum} = A \oplus B \oplus Cin \quad (1)$$

$$\text{Cout} = AB + AC_{in} + BC_{in} \quad (2)$$

GDI logic is an alternative to CMOS logic. It provides a logic function implementation with less voltage swing. The output voltage, either high or low, deviates from the threshold voltage V_t, which reduces the voltage swing by the V_{DD} (or ground). Because of this reduced voltage swing, power consumption is improved.

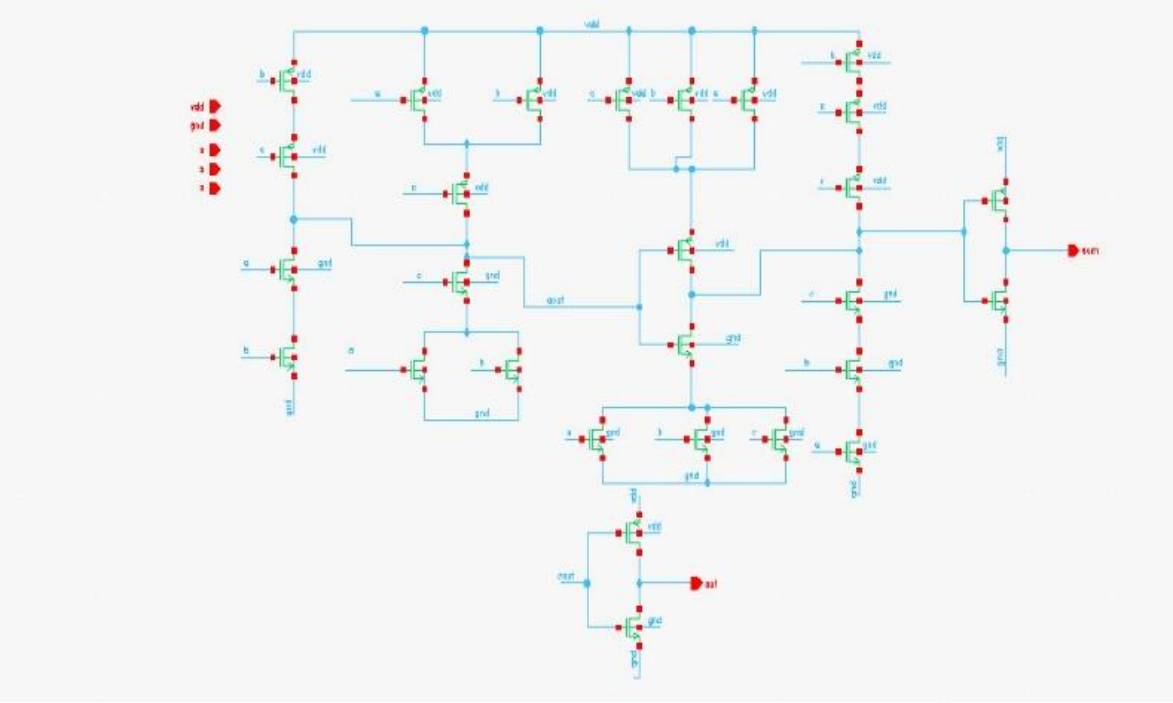

Fig. 1. 28T CMOS Full Adder circuit

However, this might lead to slow switching when cascaded operation is used.

Depending on the application, this modular architecture enables each module to be optimized for particular objectives, such as low power, fast speed, or compact space. Reducing the number of transistors can help lower power consumption.

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Various configurations have been suggested, including 14T [12], 12T, 10T, and 8T etc.[13] implementations. However, it's commonly observed that configurations with fewer than 14 transistors significantly impact the output voltage swing. This shift is usually due to how XOR is implemented, nevertheless, reducing the transistor count. This paper presents an extensive study on various low power and energy efficiency techniques for a 1-bit full adder, focusing on logic styles, hybrid digital styles, redundant components, and methods for reducing transistor count.

This work explores six proposed full adder (FA) designs: GDI1, GDI2, GDI3, GDI4, Mux based, Hybrid Full adders. The implementations are carried out using 45 nm process node using Cadence Virtuoso, with results analysed, tabulated, and compared.

2.Existing Techniques for Full adder design in Literature: A Critical Review

Full adder circuits are now much better at saving power. Researchers are making them faster and smaller too. They use smart designs like PTL, GDI, and mixed styles.

Shoba and Nakkeeran et.al [1] researched full adders using GDI. They focused on how well these adders saved energy during complex VLSI designs. Their designs used much less power than regular CMOS adders. So, they work well for low-power VLSI design.

Kamsani et al. [2] also created a full adder. It used pass transistor logic with a multiplexer. This design cut down on the number of transistors and saved energy. Their adder is a strong choice instead of standard CMOS adders. It is helpful, mostly for applications where power use is key.

K. Sanapala and R. Sakthivel [3] created a low-power full adder using GDI technology. It used less power and space. It also worked better in power use and delay.

In "Analysis of Full Adder Cells in Numerous Logic Styles," K. Murugan, R. Nithya, and others [4] examine different full adder designs. The paper compares designs using various logic styles. They focus on power use, speed, and area. The authors show how new designs improve computing. Their analysis looks at both old and new methods. This study helps researchers create efficient digital circuits. These circuits should save energy and space.

M.I. Bin Abd Majid et al.[5] looked at 8T and 10T full adders using CMOS technology. Their study showed using fewer transistors cuts power use, and gave good results.

V. M. B et al. [6] made a full adder with XNOR-XOR and DPTL. Their design sped up signals and cut leakage power. It also boosted circuit speed for fast, efficient designs.

3. Design Procedures for the Low power and energy efficiency Full adders

The CMOS full adder shown in fig.1 consists of 28 transistors, each measuring 120nm in width and 45nm in length. Simulations with a 1V supply voltage in Cadence 45 nm technology showed a power consumption of 93nW. This design occupies the most area, is prone to glitches,

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and consumes the highest power. However, its output is reliably pulled up or down, preventing floating states.

PROPOSED GDI LOGIC DESIGNS:

A basic GDI logic cell is shown in fig.2. This structure takes three inputs. N is the NMOS source. It usually connects to GND. It can also act as an input. P is the PMOS source. It usually connects to VDD. It can also act as an input. G is the gate. It controls the NMOS and PMOS transistors. The output comes from the shared drain connection. This connects both transistors. GDI cell overcomes the standard CMOS in a way to yield lower power consumption by reduced voltage swing but maintains high switching sweed.

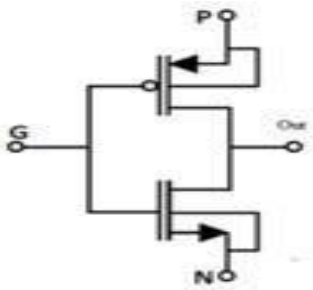

Fig.2. Basic GDI cell

GDI logic provides a good method for building simple logic gates. These gates include AND, OR, XOR, and multiplexers. An AND gate, for example, is made by linking PMOS to B. NMOS connects to GND, and Gate connects to input A. This setup results in an output of A * B. Likewise, an OR gate is created by connecting P to VDD. Then, N connects to B, and G connects to A. This creates an output of A + B. Also, XOR needs fewer transistors than CMOS when using GDI. Fig.3 shows the AND, OR and other logic gates using GDI logic.

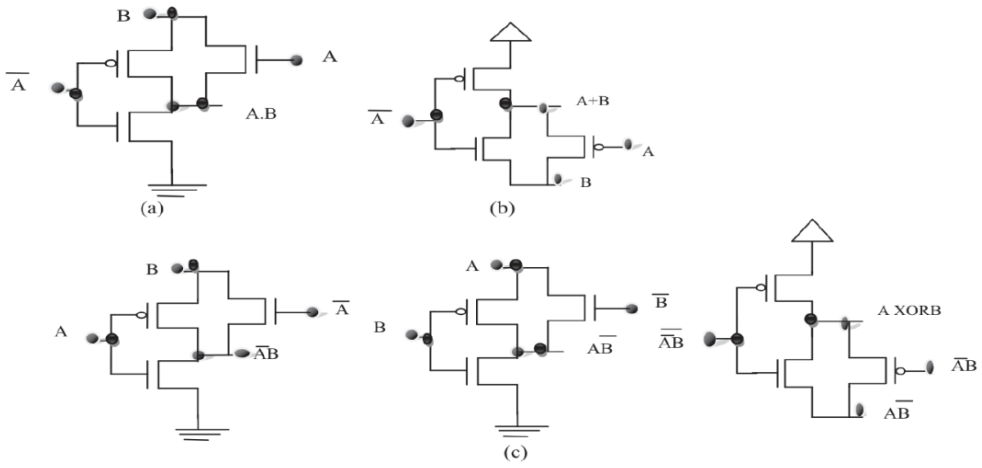

Fig.3: Logic gates using GDI

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Using GDI cells, four distinct kinds of full adders were proposed.

PROPOSED GDI BASED FULL ADDER-1

Each of the 18 transistors in the first design shown in fig.4 has a width of 120 nm and a length of 45 nm. A 1V supply voltage in Cadence 45 nm technology was employed in the simulations. The sum and carry-out equations are extended in this design. The sum output can be generated by regulating the XOR and its opposite (XNOR) functions via the input Cin. Using the XOR of inputs A and B as select lines for multiplexed inputs A and Cin, the carry-out (C_{out}) is produced. Equations (5) and (6) were implemented in this design.

$$\text{Sum} = C_{in} \cdot (A \oplus B) + C_{in} \cdot (A \oplus B) \qquad (3)$$

$$C_{out} = (A \oplus B) \cdot C_{in} + (A \oplus B) \cdot A \qquad (4)$$

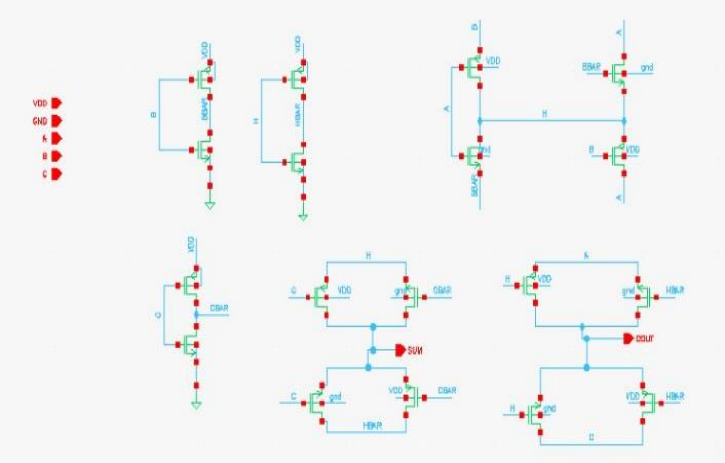

Fig.4. GDI 1 based full adder circuit

PROPOSED GDI BASED FULL ADDER-2*:*

The second design of the full adder shown in fig.5 uses equations (5) and (6). It has 22 transistors, each measuring 120 nm in width and 45 nm in length. The simulations used a supply voltage of 1V in Cadence 45 nm technology. The carry-out (C_{out}) is made using intermediate results from AND and OR operations of inputs A and B. These intermediate results are then controlled by the input Cin, which functions as a select line to generate the final output. Equations (7) and (8) were used for the implementation.

$$\text{Sum} = A \oplus B \oplus C_{in} \qquad (5)$$

$$C_{out} = C_{in} \cdot (A \cdot B) + C_{in} \cdot (A + B) \qquad (6)$$

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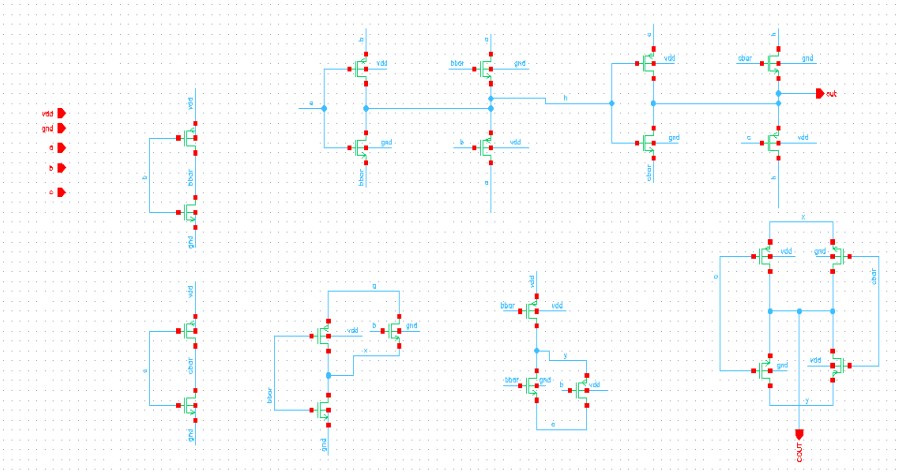

FIG. 5. GDI 2 based full adder circuit

PROPOSED GDI BASED FULL ADDER-3*:*

The GDI 3 design shown in fig.6 uses 23 transistors, with dimensions of 120 nm in width and 45 nm in length. The simulations were conducted with a 1V supply voltage in Cadence 45 nm technology. Logical gates such as AND, OR, and XOR are employed to compute the carry-out (C_{out}). Equations (7) and (8) were implemented in this design.

$$\text{Sum} = A \oplus B \oplus C_{in} \tag{7}$$

$$C_{out} = (A \cdot B) + C_{in} \cdot (A \oplus B) \tag{8}$$

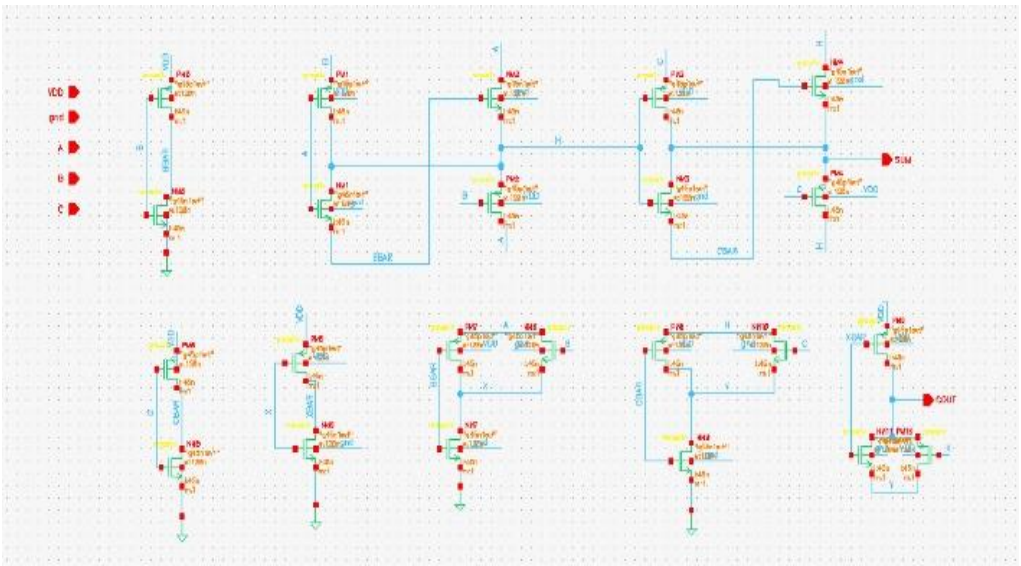

FIG. 6. GDI 3 based full adder circuit

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PROPOSED GDI BASED FULL ADDER-4*:*

The GDI 4 design shown in fig.7 includes a total of 14 transistors, each with specified dimensions, as shown in Table I. This design comprises the following logical blocks:

- A single XOR/XNOR block
- Two multiplexers
- Restored Transmission Gate with One Swing (SRTG)
- A block of single-swing restored pass transistors (SRPT)

Equations (9) and (10) were used for the implementation of the sum, carry-out (C_{out}).

$$\text{Sum} = C_{in}(A \oplus B) + C_{in}(A \oplus B) \quad (9)$$

$$C_{out} = (A \cdot B) + C_{in}(A \oplus B) \quad (10)$$

TABLE I. Transistor dimensions in GDI based full adder-4 design

Transistor	Width (nm)	Length (nm)
PM0, PM2	240	45
PM1, PM3	360	45
PM5	480	45
PM4, PM6	120	45
NM0 to NM6	120	45

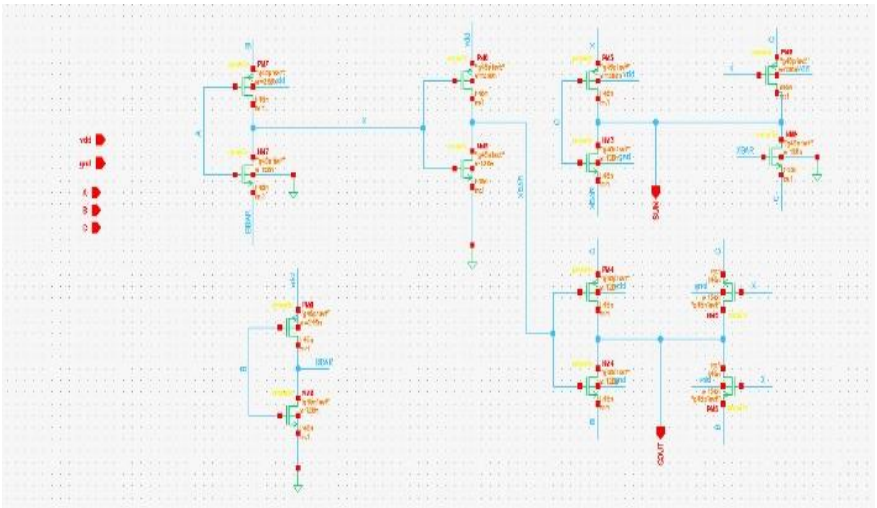

Fig. 7. GDI 3 based full adder circuit

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PROPOSED MUX BASED FULL ADDER

An implementation based on a multiplexer (MUX) and employing 22 transistors has transistors that are 120 nm width and 45 nm length. Together, these transistors enable the circuit's effective signal routing. With a 1V supply voltage, the system is made to function within the ideal power limits for sophisticated electronic applications. The MUX can carry out intricate logical processes while consuming less power and improving overall circuit performance thanks to the transistors' small size, which permits high-density integration. This MUX's voltage supply and selected dimensions ensure a balance between energy efficiency and functionality, making it appropriate for contemporary, low-power electronic devices. Implementation of MUX based Full adder in Cadence 45nm technology is shown in Fig.8.

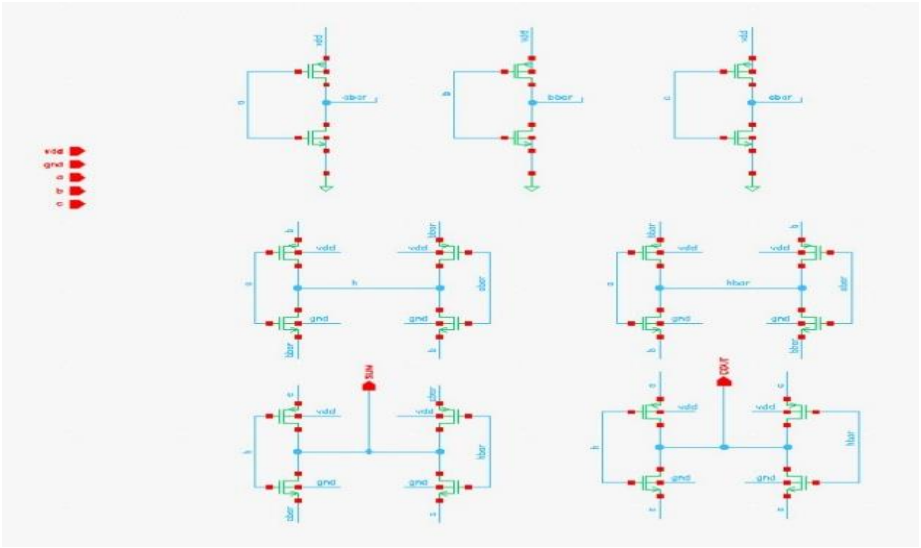

Fig. 8. Mux based Full adder

PROPOSED HYBRID FULL ADDER :

This very efficient hybrid full adder design uses an 8 transistor (8T) arrangement for both the XOR and XNOR gates in its module. This approach is more compact and powerefficient than traditional designs because it uses fewer transistors. Whereas the XNOR gate generates a high output when the inputs are the same, the XOR gate generates a high output when the inputs are different. Through the integration of several logic styles and components, including swing restored gates, multiplexers, and GDI cells, the whole adder strikes a balance between area, power, and speed. For situations where power and space are important factors, the addition of 8T XOR and XNOR gates produces a more effective and efficient design. Implementation of Hybrid Full adder in Cadence 45nm technology is shown in Fig.9.

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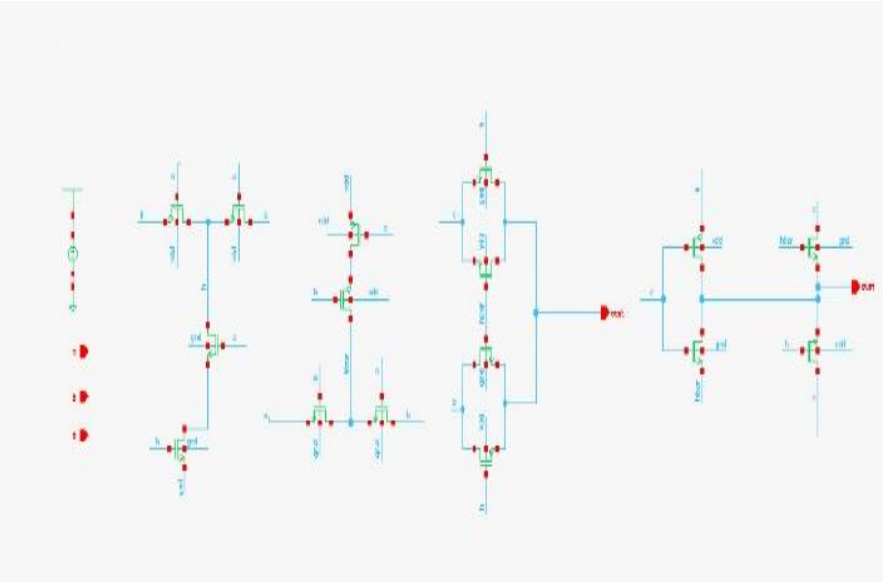

Fig.9. Hybrid Full Adder

4.SIMULATION RESULTS

This part presents the simulation results of the proposed six Full adder designs. These designs were evaluated based on power consumption, propagation delay, transistor count, and power-delay product (PDP) or energy shown in TableII to assess their efficiency against conventional CMOS full adder. All simulations were conducted using Cadence Virtuoso with a 45nm CMOS technology node and a 1V power supply under identical test conditions. Fig.10, 11 show the comparison of power consumption and propagation delay of all proposed six designs with the existing CMOS Full adder. Fig.12, 13,14,15,16, and 17 show the input and output waveforms of proposed GDI1, GDI2, GDI3, GDI4, Mux based, Hybrid Full adders.

TABLE II performance comparison of full adder designs

Technique	Power (nW)	Delay =*(10^-9) s	PDP= *(10^-18) J	No of Transistors
CMOS FA [Existing]	93	0.16	14.88	28
MUX FA [proposed]	72.7	0.5	36.35	22
GDI 1 FA [proposed]	66.8	14.1	941.8	18
GDI 2 FA [proposed]	84.5647	0.184	15.5400048	22
GDI 3 FA [proposed]	95.18	14.2	1351.556	23
GDI 4 FA (14 T) [proposed]	103.88	23	2369	14
16T HYBRID FA [proposed]	41.9695	0.0213	0.89385135	16

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Fig.10. Comparison of Power consumption of adders

Fig.11. Comparison of Delay Analysis of adders

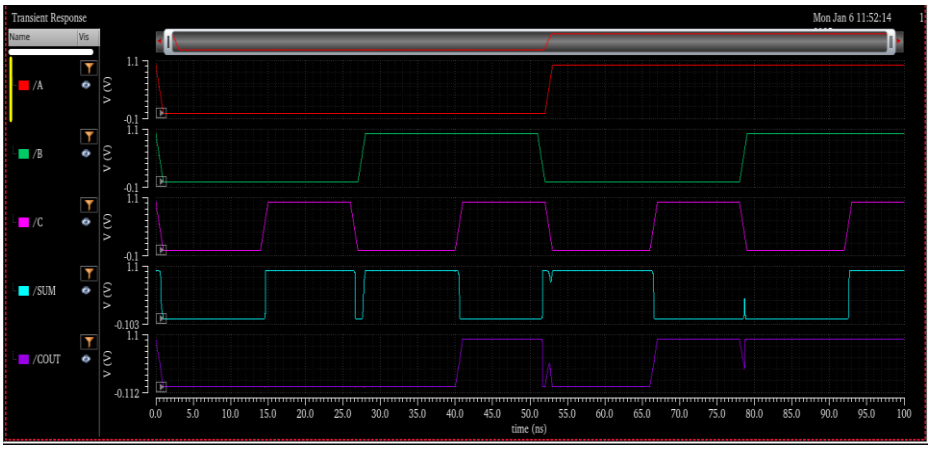

Fig.12: GDI 1 Based Full Adder Input& Output Waveforms

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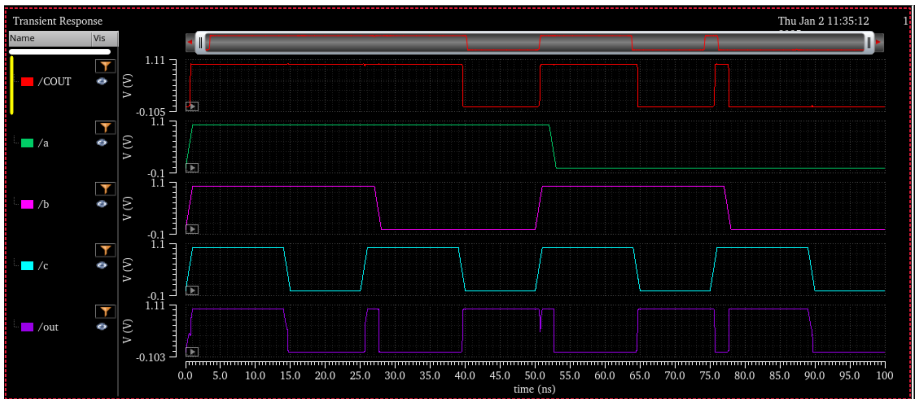

Fig.13: GDI 2 Based Full Adder Input& Output Waveforms

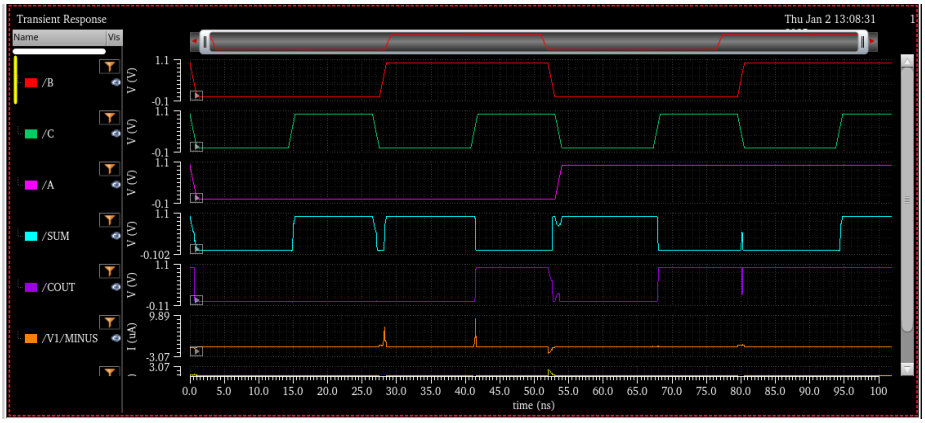

Fig.14: GDI 3 Based Full Adder Input& Output Waveforms

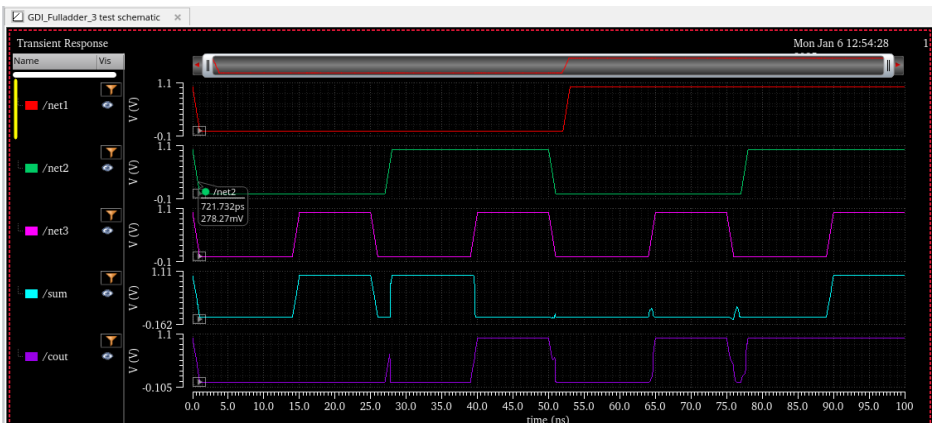

Fig.15: 14T GDI 4 Based Full Adder Input& Output Waveforms

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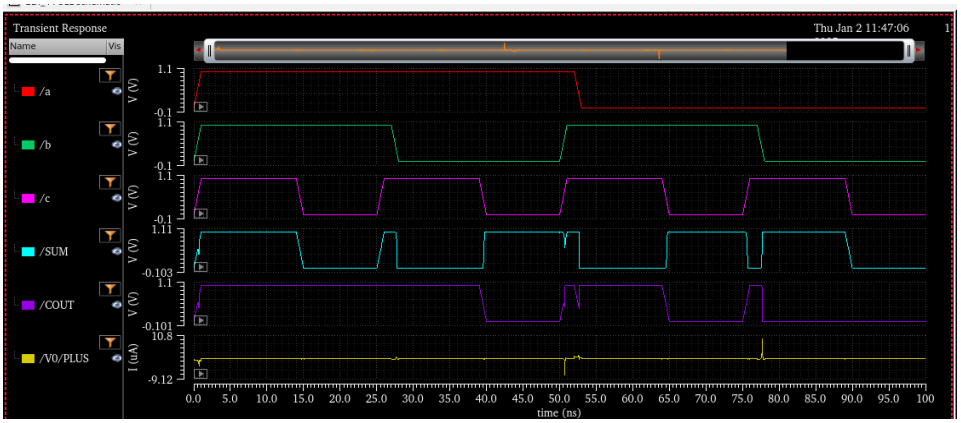

Fig.16: MUX Based Full Adder Input& Output Waveforms

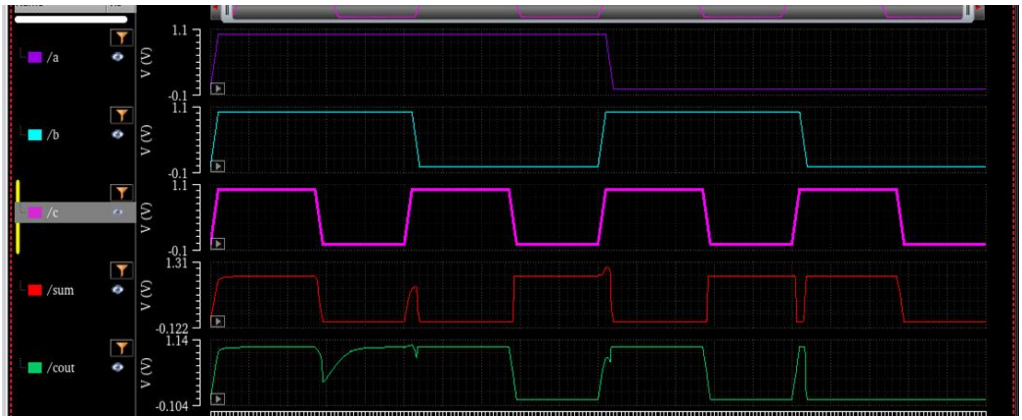

Fig.17: 16T HYBRID Full Adder Input& Output Waveforms

5. Discussions & Observations

GDI 1 FA: This design achieves a low power consumption of 66.8 nW. However, the delay of 14.1 ns results in a high PDP of 941.88 × 10^{-18} J, making it less suitable for high-speed applications.

GDI 2 FA: With a power consumption of 84.5 nW and a significantly lower delay of 0.18 ns, the PDP of 15.22 × 10^{-18} J highlights its efficiency for energy efficiency and high-speed operations.

GDI 3 FA: Although GDI 3 has a power consumption of 95.18 nW, its high delay of 14.2 ns results in a PDP of 1351.56 × 10^{-18} J, making it less efficient than GDI 2.

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GDI 4 FA: The 14T GDI4 design exhibits the highest power consumption of 169.96 nW and a delay of 24 ns, leading to a PDP of 4079.04× 10^{-18} J. This makes it the least efficient among all the designs.

MUX-Based Full Adder: The MUX-based implementation demonstrates significant power savings with a consumption of 72.7 nW and a delay of 0.50 ns. The PDP(energy) of 36.35×10^{-18} J makes it an efficient choice for applications requiring energy efficiency and low power consumption.

16T Hybrid Full Adder : The 16T Hybrid FA design achieves outstanding performance with a power consumption of 41.96 nW, a delay of 0.0213 ns, and a PDP of 0.89 × 10^{-18} J. This design is highly suitable for applications that require low power, energy efficiency and high speed, setting it apart from other implementations.

The analysis highlights the 16T Hybrid FA as the most efficient design, excelling in all key metrics. The MUX-based and GDI 2 designs also show competitive performance, while traditional CMOS and GDI 3 lag behind due to their higher PDP values.

6.Conclusions

This paper presents the design and detailed transistor level implementations of five full adders in Cadence 45nm CMOS technology. This shows implementations of various full adders using different techniques such as conventional CMOS, GDI, Mux based and Hybrid techniques. The 16T Hybrid FA design stands out as the most efficient in terms of power, delay, and PDP. MUX-based and GDI1, GDI 2 implementations also show favourable results compared to traditional CMOS designs. Future work may explore the possibility of implementing the better techniques for energy efficient full adders using hybrid styles and also incorporate the process, voltage and temperature variations on them and may build variation resilient designs.

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