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Small Signal Stability based Controller Tuning for Enhanced LVRT Performance of VSC-HVDC Transmission System

Nargunadevi TS, Anbuselvi SV, Kumudini Devi RP

Department of Electrical and Electronics Engineering, College of Engineering Guindy, Anna University, Chennai, India

Abstract: - This paper proposes an optimization based tuning technique for a two-terminal Voltage Source Converter based High Voltage Direct Current (VSC-HVDC) transmission system with a Modified Reactive Power Controller (MRPC). Latency in controller switching and gain modulation is avoided by employing MRPC controller. Reactive power reference modulation strategy is employed to provide optimal Low Voltage Ride Through (LVRT) support. The state space model is derived and initialized from steady state operating conditions prior to the onset of dynamic behavior of the system. The critical modes are identified. From the normalized participation factor matrix, the LVRT sensitive modes and the DC voltage sensitive modes are identified. The objective function of the optimization technique is to enhance the stability and damping, prioritizing LVRT support and reduction of DC bus voltage oscillations. Comprehensive Simulation studies are done using PSCAD/EMTDC. On occurrence of fault or low voltage pocket, the improved performance of the proposed tuning technique over traditional tuning for various operating conditions is demonstrated.

Keywords*:* Enhanced Low Voltage Ride Through, Modified Reactive power controller, Voltage sensitive modes, Optimization based tuning, Dynamic modeling of Voltage Source Converter based High Voltage Direct Current system.

1. Introduction

With ever increasing non-conventional generations and loads penetrating into the grid, stability enhancement of the grid is challenged. VSC based DC transmission systems have gained popularity in evacuating bulk power from renewable energy generating sources such as offshore wind power generators, solar power generators, etc., Unlike conventional AC system, VSC Multi Terminal Direct Current (MTDC) system has the four-quadrant operation capability and independent dq control capability. VSC MTDC systems can be employed for better transfer capabilities under weak grid conditions which is more prevalent in wind power evacuation systems [1]. VSC HVDC system can enhance grid stability [2] and provide inertia support to the interconnected AC system and enhanced Fault Ride Through (FRT) capability [3].

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Wind power potential is abundant in remote geographical locations where grid is usually weak and low voltage pockets are anticipated [4]. LVRT conditions are invoked when significant voltage drop on the AC system is detected followed by DC link voltage oscillations. The reactive power pumped by the VSC –HVDC link is increased to meet the reactive power requirement of the system during ride through period [5]. During the ride-through period the wind power is evacuated more as reactive power rather than real power to the grid as the objective is to remain connected to the grid. Maximum reactive power support capability of VSC- HVDC system can be extracted by dynamically adjusting active and reactive current references [6]. Trade-off is arrived between adjusting real power droop setting and LVRT support without violating device current limitations [7].

Many literatures have proposed various control strategies for LVRT ride through enhancement of VSC based HVDC intertie connecting wind power generators. The rate at which the energy stored in the DC link capacitor is freewheeled, depends on the maximum device current limitation and di/dt stress withstand capability of the device, which is different for VSC and MMC converters of vivid topologies [8]. Coordination among the sending and receiving end converter controllers is suggested by sensing the DC capacitor voltages to avoid latency in communication [9]. It is obvious that disruptive over voltages across DC capacitors can be anticipated when the power pooled into DC network could not be evacuated due to faults on AC side. Sequentially dissipating the energy stored in DC link capacitors of VSC HVDC link and dissipation of distributed energy stored in DC link capacitors of DFIG or PMSG based wind turbine generators are adapted [4].

The dynamics of fast inner current controllers and outer controllers are generally focused in small signal stability based tuning methodologies reported in various literatures [10]-[12]. The interaction modes of the VSC MTDC system is identified and analysed to differentiate between controller modes, DC system modes and AC system modes [10]. The PLL dynamics plays a vital role, the wider bandwidth of the PI controller corresponding to faster dynamics is detrimental to the stability of the system [12]. Eigen value sensitivity based tuning methodologies are conventionally adopted for both VSC-MTDC system [13] and LCC-VSC Hybrid systems [14]. Extended participation factor matrices are computed for various initial operating conditions at the onset of dynamic behaviour of the system [13]. The objective of tuning is to maximize the overall stability of the system [14]. A quadratic sub-optimal index of output feedback is used to evaluate the system stability. [15] Time domain metrices are used for optimizing the control parameters using EMT model of the system and the influence of various gain parameters on various modes gives an in-depth insight of the controller dynamics [16].

Emphasis on LVRT enhancement using small signal stability analysis-based optimization tuning employing MRPC (Modified Reactive Power Controller) has not been addressed. In this

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paper, eigen value sensitivity-based optimization methodology is used for tuning the gain parameters of the VSC-HVDC system with modified reactive power controller. The organization of this paper is as follows: Section 2 briefs about the dynamic modeling of the VSC-HVDC link including the DC System and the controllers adopted from [2]. The AC system equations are adopted from [17]. Section 3 discusses the identification of LVRT sensitive modes and DC voltage sensitive modes, traditional tuning methodology and sensitivity based tuning methodology. Section 4 discusses stability of the system with respect to variation in various gain parameters and the simulation of the system under study using PSCAD/EMTDC and the results.

2. Dynamic Modeling of VSC-HVDC Link

The objective of this paper is focused on LVRT capability enhancement offered by a VSC HVDC system. In cases where HVDC link is deployed for offshore wind power evacuation, LVRT capability becomes more significant rather than frequency support. Assuming that the system has got sufficient spinning reserves to provide inertial support, the considered HVDC link focuses only on LVRT support.

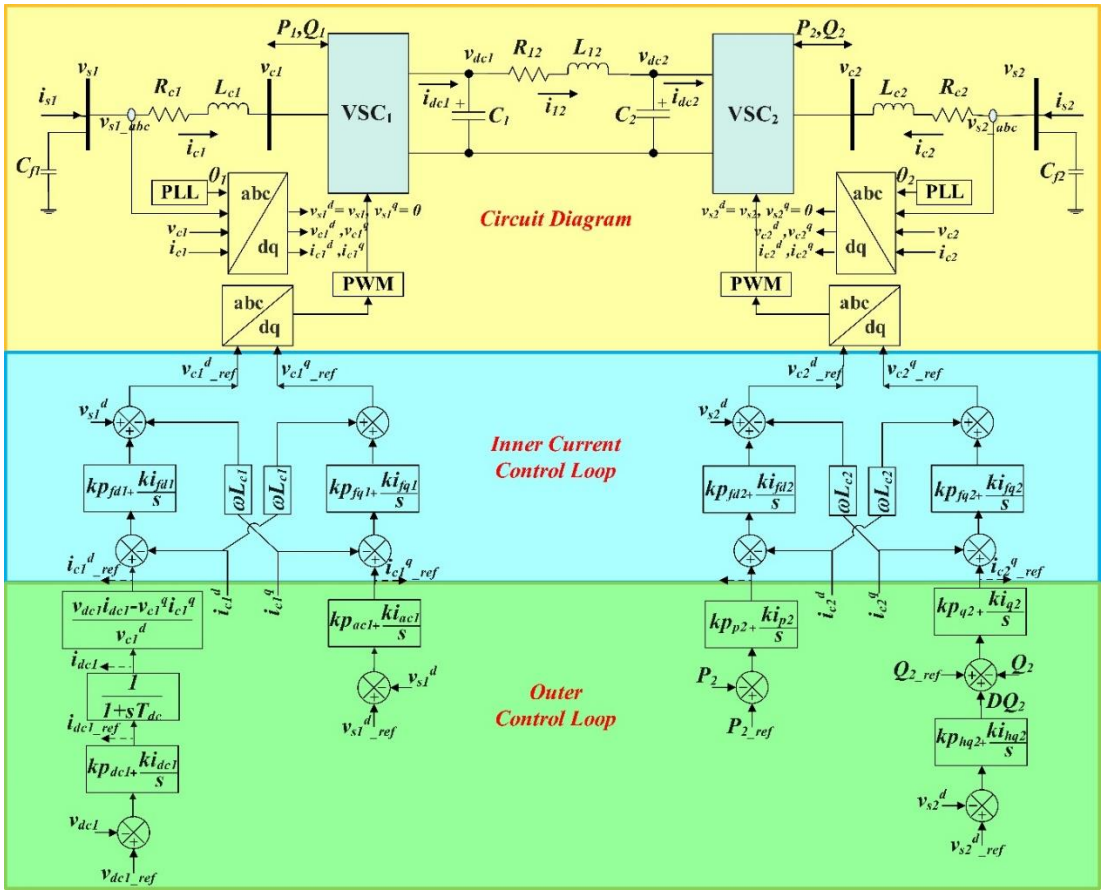

Fig. 1. Overall Block Diagram of the VSC-HVDC Transmission System

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In this paper, a conventional grid voltage vector orientation control is adapted with q axis leading the d axis and the voltage phasor at the Point of Common Coupling (PCC) is aligned with the d-axis. The small signal model of two terminal VSC-HVDC link is derived from the set of dynamic equations pertaining to AC network, DC link and the controllers. The equations are linearized around an initial operating steady state condition obtained from PSCAD/EMTDC simulation.

The model of the AC system adopted in the study of VSC HVDC is conventionally the thevenin equivalent of the power system connected to the PCC with the filter capacitor connected at PCC. The current flow through thevenin equivalent reactance and PCC voltage are depicted as state variables pertaining to AC system in the dq component form. Fig. 1 shows the overall block diagram of the system under study with all the controllers.

The reference frame orientation adopted in this paper is d axis leading the q axis and the d axis is aligned with the grid voltage, where $v_s^d = v_s;\ v_s^q = 0$. Hence the decoupled real and reactive power equations are taken as $P = v_s^d * i_c^d \ and \ Q = v_s^d * i_c^q$.

2.1. Modeling of the AC System

From Fig. 1, the power system and the VSC HVDC converters are connected by an impedance $Z_{cn} = R_{cn} + jX_{cn}$, where n=1 for AC system 1 and n=2 for AC system 2. The circuit equation can be written as

$$v_{sn} - v_{cn} = R_{cn} i_{cn} + L_{cn} \frac{di_{cn}}{dt} \tag{1}$$

$$L_{cn} \frac{di_{cn}}{dt} = v_{sn} - v_{cn} - R_{cn} i_{cn} \tag{2}$$

$$C_{fn} \frac{dv_{sn}}{dt} = i_{sn} - i_{cn} \tag{3}$$

The dynamic equations can be transformed to a rotating dq reference frame which is synchronized with the grid voltage,

$$\frac{di_{cn}^d}{dt} = -\frac{R_{cn}}{L_{cn}} i_{cn}^d - \omega i_{cn}^q + \frac{1}{L_{cn}} v_{sn}^d - \frac{1}{L_{cn}} v_{cn}^d \tag{4}$$

$$\frac{di_{cn}^q}{dt} = \omega i_{cn}^d - \frac{R_{cn}}{L_{cn}} i_{cn}^q - \frac{1}{L_{cn}} v_{cn}^q \tag{5}$$

$$\frac{dv_{sn}^d}{dt} = \frac{1}{c_{fn}} (i_{sn}^d - i_{cn}^d) \tag{6}$$

A total of 6 equations represent the AC system from both sides. The equations (4) – (6) are used to model the dynamic equations of the AC systems 1 and 2.

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2.2. Modeling of the DC system

The DC system is modeled using lumped parameters. The dynamic equations of the DC system are

$$C_{dc}\frac{dv_{dc1}}{dt} = i_{dc1} - i_{12} \tag{7}$$

$$C_{dc}\frac{dv_{dc2}}{dt} = i_{dc2} + i_{12} \tag{8}$$

$$L_{dc}\frac{di_{12}}{dt} = v_{dc1} - v_{dc2} - R_{dc}i_{12} \tag{9}$$

where i_{dc2} is an linearized algebraic variable obtained from the power balance equation $P_{ac} = P_{dc}$

$$i_{dc2} = \frac{\left(v_{c2}^{d}i_{c2}^{d} + v_{c2}^{q}i_{c2}^{q}\right)}{2v_{dc2}} \tag{10}$$

2.3. Modeling of the controller

Dynamic gain modulation and controller switching, though prevalent in controller design is not employed in this work. Latency in controller switching and gain modulation is avoided by MRPC controller. In the vector current control method, by aligning the d axis with the grid voltage v_{sn}, the component along q axis is made equal to zero. Thus decoupled control is achieved by varying i_{cn}^{d} to control real power and varying i_{cn}^{q} to control reactive power.The controllers are modeled considering DC Link Voltage controller and AC bus voltage controller in converter 1 and Real and Reactive power controllers in converter 2.

$$P_n = v_{sn}^{d} * i_{cn}^{d} \tag{11}$$

$$Q_n = v_{sn}^{d} * i_{cn}^{q} \tag{12}$$

2.3.1. DC Link Voltage Controller

The output of the outer PI controller pertaining to DC link voltage control is taken as i_{dc1_ref} rather than $i_{c1_{ref}}^{d}$ to enhance the bandwidth of the controllers. The DC link voltage is directly proportional to the corresponding i_{dc1} current.

$$i_{dc1_{ref}} = \left(kp_{dc1} + \frac{ki_{dc1}}{s}\right)\left(v_{dc1_{ref}} - v_{dc1}\right) \tag{13}$$

$$N_{dc1} = \frac{ki_{dc1}}{s}\left(v_{dc1_{ref}} - v_{dc1}\right) \tag{14}$$

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From the equation i_{dc1_ref} , the DC current can be obtained by including a time constant T_{dc}, which corresponds to the dynamics of the DC circuit.

$$i_{dc1} = \left(\frac{1}{1+sT_{dc}}\right) i_{dc1\_ref} \tag{15}$$

$i^d_{c1\_ref}$ is algebraically calculated from i_{dc1} from equation (16) using the power balance equation, $P_{ac} = P_{dc}$. When compared to the DC Link Voltage controller, this formulation widens the bandwidth to regulate the DC bus voltage.

$$i^d_{c1\_ref} = \left(\frac{v_{dc1} i_{dc1} - v^q_{c1} i^q_{c1}}{v^d_{c1}}\right) \tag{16}$$

The output of the inner current control loop is then found and a time constant T, is introduced which is the time delay between the actual value and the reference value of the voltage due to the converter's power electronics.

$$v^d_{c1\_ref} = v^d_{s1} + \left(\left(kp_{fd1} + \frac{ki_{fd1}}{s}\right)\left(i^d_{c1\_ref} - i^d_{c1}\right)\right) - \omega L_{c1} i^q_{c1} \tag{17}$$

$$M_{dc1} = \frac{ki_{fd_1}}{s}\left(i^d_{c1\_ref} - i^d_{c1}\right) \tag{18}$$

$$v^d_{c1} = \left(\frac{1}{1+sT}\right) v^d_{c1\_ref} \tag{19}$$

The outer controller of the DC bus voltage regulating converter or the slack converter is modified to fully represent the power balance of AC/DC interactions. The output of PI controller is taken as DC current reference, rather than $i^d_{c1\_ref}$, which is computed algebraically using power balance equation as shown in the equation (16). This significantly enhances the stability of the LVRT performance.

2.3.2. AC Bus Voltage Controller

The AC bus voltage is directly proportional to the q-axis component of the converter current. Hence the ac bus voltage can be controlled by varying i^q_{cn}. The outer control loop equation is

$$i^q_{c1\_ref} = \left(kp_{ac1} + \frac{ki_{ac1}}{s}\right)\left(v^d_{s1\_ref} - v^d_{s1}\right) \tag{20}$$

$$N_{ac1} = \frac{ki_{ac1}}{s}\left(v^d_{s1\_ref} - v^d_{s1}\right) \tag{21}$$

The inner control loop equations are

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$$v_{c1\_ref}^{q} = \left(\left(kp_{fq1} + \frac{ki_{fq1}}{s}\right)\left(i_{c1\_ref}^{q} - i_{c1}^{q}\right)\right) + \omega L_{c1} i_{c1}^{d} \tag{22}$$

$$M_{ac1} = \frac{ki_{fq1}}{s}\left(i_{c1_{ref}}^{q} - i_{c1}^{q}\right) \tag{23}$$

$$v_{c1}^{q} = \left(\frac{1}{1+sT}\right) v_{c1\_ref}^{q} \tag{24}$$

2.3.3. Real Power Controller

The real power is directly proportional to the d-axis component of the converter current. Hence the real power can be controlled by varying i_{c2}^{d}.

$$i_{c2\_ref}^{d} = \left(kp_{p2} + \frac{ki_{p2}}{s}\right)\left(P_{2\_ref} - P_{2}\right) \tag{25}$$

$$N_{p2} = \frac{ki_{p2}}{s}\left(P_{2\_ref} - P_{2}\right) \tag{26}$$

The inner current control loop then calculates the converter voltage accordingly.

$$v_{c2\_ref}^{d} = v_{s2}^{d} + \left(\left(kp_{fd2} + \frac{ki_{fd2}}{s}\right)\left(i_{c2\_ref}^{d} - i_{c2}^{d}\right)\right) - \omega L_{c2} i_{c2}^{q} \tag{27}$$

$$M_{p2} = \frac{ki_{fd2}}{s}\left(i_{c2\_ref}^{d} - i_{c2}^{d}\right) \tag{28}$$

$$v_{c2}^{d} = \left(\frac{1}{1+sT}\right) v_{c2\_ref}^{d} \tag{29}$$

2.3.4. Modified Reactive Power Controller

The VSC converter can either have reactive power controller or AC bus voltage controller. The converter with reactive power controller can only provide a fixed contribution to voltage regulation of the AC bus, whereas dynamic contribution is required to improve the voltage profile. The dynamic equation of the modified reactive power controller which also takes into account the variation in the AC bus voltage is given below.

$$DQ_2 = \left(kp_{hq2} + \frac{ki_{hq2}}{s}\right)\left(v_{s2\_ref}^{d} - v_{s2}^{d}\right) \tag{30}$$

$$H_{q2} = \frac{ki_{hq2}}{s}\left(v_{s2\_ref}^{d} - v_{s2}^{d}\right) \tag{31}$$

DQ_2 is the amount of reactive power provided by the converter, proportional to the change in the AC bus voltage, which is limited by the converter MVAR limitation.

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$$i_{c2\_ref}^{q} = \left(kp_{q2} + \frac{ki_{q2}}{s}\right)\left(Q_{2\_ref} + DQ_2 - Q_2\right) \tag{32}$$

$$N_{q2} = \frac{ki_{q2}}{s}\left(Q_{2\_ref} + DQ_2 - Q_2\right) \tag{33}$$

The reactive power is directly proportional to the q-axis component of the converter current. Hence the reactive power can be controlled by varying i_{c2}^{q}.

$$v_{c2\_ref}^{q} = \left(\left(kp_{fq2} + \frac{ki_{fq2}}{s}\right)\left(i_{c2\_ref}^{q} - i_{c2}^{q}\right)\right) + \omega L_{c2} i_{c2}^{d} \tag{34}$$

$$M_{q2} = \frac{ki_{fq2}}{s}\left(i_{c2\_ref}^{q} - i_{c2}^{q}\right) \tag{35}$$

$$v_{c2}^{q} = \left(\frac{1}{1+sT}\right) v_{c2\_ref}^{q} \tag{36}$$

The limits for the reference currents during fault are $\left[i_{c2\_ref\_fault}^{q}\right]_{i_{c2\_ref}^{q}}^{i_{c2\_max}}$ and $\left[i_{c2\_ref\_fault}^{d}\right]_{0}^{i_{c2\_ref}^{d}}$ to satisfy the device current limitation.

3. Small Signal Stability based Tuning

Small signal stability-based tuning is used to co-ordinately tune the gain parameters. Co-ordinated tuning is essential when many controllers are cascaded, to ensure closed loop stability. The dynamic equations are linearized around the initial operating point obtained from the steady state results of Power Flow Analysis. From the dynamic equations, the state matrix is formulated. Initialization of A matrix is performed using an initial steady state obtained before the onset of dynamic oscillations and the eigen values are computed. Linearization of the state space equations are not valid during dynamic period. But the steady state operating point prior to commencement of disturbance is considered for initialization. Although linearized model is not strictly accurate it gives a better insight into the dynamic coupling among modes and the state variables [18].

The critical modes are identified. The state variables pertaining to the AC System 1 are $i_{c1}^{d}, i_{c1}^{q}, v_{s1}^{d}$. The variables $i_{c2}^{d}, i_{c2}^{q}, v_{s2}^{d}$ corresponds to the AC System 2. The variables of the DC System are $v_{dc1}, v_{dc2}, i_{12}, i_{dc1}$ where i_{12} is the DC current between converters 1 and 2 and i_{dc1} is the slack converter current.

The state variables pertaining to the controllers are grouped into four, pertaining to VSC1 and VSC2. $N_{dc1}, M_{dc1}, v_{c1}^{d}, i_{c1}^{d}, v_{dc1}, i_{dc1}$ are the state variables for DC Link Voltage controller and $N_{ac1}, M_{ac1}, v_{c1}^{q}, v_{s1}^{d}, i_{c1}^{q}$ are the state variables for AC Voltage regulator, pertaining to VSC1.

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The state variables for Real Power controller are $N_{p2}, M_{p2}, v_{c2}^{d}, v_{s2}^{d}, i_{c2}^{d}$ and the state variables for Modified Reactive Power controller are $H_{q2}, N_{q2}, M_{q2}, v_{c2}^{q}, v_{s2}^{d}, i_{c2}^{q}$.

Table 1. Eigen values and percentage participation of state variables – Initial Steady state

Mode No.	Eigen value	Frequency	Damping ratio	Percentage participation of State variables
1,2	-53.3384 ± 1203.1735i	191.49	0.04	i_{c1}^{q} - 48.16 M_{ac1} - 4.00 v_{c1}^{q} - 47.84
3,4	-94.2097 ± 2290.0278i	364.47	0.04	i_{c2}^{q}- 49.80 v_{c2}^{q} - 49.78
5	-993.6774 + 0i	0	1.00	i_{dc1} - 99.37
6,7	-102.6584 ± 67.1302i	10.68	0.84	i_{c1}^{d} - 29.53 v_{s1}^{d} - 25.12 v_{c1}^{d} - 45.25
8	-100.6692 + 0i	0	1	M_{ac1} - 98.35
9,10	-101.2728 ± 118.0995i	18.8	0.65	i_{c2}^{d} - 39.39 v_{s2}^{d}- 20.22 v_{c2}^{d} - 40.35
11,12	-20.0969 ± 70.2787i	11.19	0.27	v_{dc1} - 27.49 v_{dc2} - 22.51 i_{12} - 49.82
13,14	-1.3679 ± 4.6060i	0.73	0.28	i_{c1}^{d} - 3.05 v_{s1}^{d} - 8.87 v_{c1}^{d} - 40.17 N_{ac1} - 47.74
15	-33.1953 + 0i	0	1	v_{c2}^{q} - 36.83 v_{dc2} - 53.50 i_{12} - 9.40
16,17	-2.3869 ± 4.8107i	0.77	0.44	i_{c2}^{d} - 2.08 v_{s2}^{d} - 23.29 v_{c2}^{d} - 24.70 H_{q2} - 46.14 N_{q2} - 3.47

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18	-10.0086 + 0i	0	1.00	M_{q2}- 99.05
19	-8.8510 + 0i	0	1.00	H_{q2} - 5.25 N_{q2} - 93.64
20	-0.0123 + 0i	0	1.00	N_{dc1} - 99.94
21	-5.9665 e-05 + 0i	0	1.00	M_{dc1} - 99.97
22	-1.1918 e-14 + 0i	0	1.00	H_{q2} - 100.00
23	-6.3425 e-05 + 0i	0	1	N_{p2} - 33.28 M_{p2} - 33.47 H_{q2} - 33.26

Eigen value analysis is done to study the small signal stability of the system. Table 1 lists the eigen values and their corresponding frequencies and damping ratios of the system for the initial steady state operating point. The critical modes are modes 20, 21, 22 and 23. Among them mode 22 is the most critical mode since it is very close to the imaginary axis. The participation matrix is formulated to understand the participation of various state variables in every mode and the change in their participation as the value of gain parameters vary. In Mode n, the participation of the state variables corresponding to MRPC is significant. In Mode m, the participation of the state variables corresponding to DC voltage controller is significant. The state variables with participation less than 1 percentage are omitted from the Table 1.

3.1. Mode Identification

The participation of the state variables pertaining to LVRT modes are identified from the normalized participation factor matrix. The 3 cascaded controllers controlling the q-axis current i_{c2}^{q} of converter 2 as shown in Fig. 1, is named as MRPC. In MRPC, the outermost loop generates DQ_2, a modulation signal proportional to AC voltage error. A limiter is deployed to limit DQ_2 to zero when AC voltage error is insignificantly small. It is observed from Table 1, that modes 3, 4, 15, 16, 17, 18, 19, 22 and 23 are LVRT sensitive modes as participation of the state variables $H_{q2}, N_{q2}, M_{q2}, v_{c2}^{q}, v_{s2}^{d}, i_{c2}^{q}$ of the MRPC are found to be significant in them and modes 5, 6, 7, 13, 14, 20 and 21 are found to be DC voltage controller modes as participation of the state variables $N_{dc1}, M_{dc1}, v_{c1}^{d}, i_{c1}^{d}, v_{dc1}, i_{dc1}$ are found to be significant in them. Each gain parameter is subjected to parameter perturbation from minimum to maximum within the pre-set bounds, for different initial conditions and a set of A matrices are obtained and the corresponding eigen values are obtained. The impact of varying the various gain parameters on the stability of the system is analysed.

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3.2. Small Signal Stability based on Existing Tuning method

The initial step of the existing tuning method is identification of the critical modes. The critical modes (modes 20 to 23) are given higher priority while tuning. The critical modes are first in order of the tuning sequence. The effect of gain parameters on the stability of the modes is studied by varying each proportional and integral gain within specified limits, while the other gain parameters are considered constant. Using the above procedure, sequentially the modes are tuned. A trade-off has been implemented so that the previously stable modes are not destabilized. The bounds for all the gain parameters on the search space are defined.

The objective function of the optimization-based tuning is formulated to maximize small signal stability indices of the system. The objective function of the existing tuning method is

$$Objectivefunction = min \sum_{i=1}^{m} \{W_{si} * (\sigma_i - \sigma_0)^2\} + min \sum_{i=1}^{m} \{W_{di} * (\zeta_0 - \zeta_i)^2\} \quad (37)$$

where, $W_{si} = 1/\sigma_i$, weighing factor assigned to ith mode

$W_{di} = 1/\zeta_i$, weighing factor assigned for damping of ith mode

σ_i - real part of ith mode

σ_0- centroid of the critical mode

ζ_i - damping ratio of ith mode

ζ_0 - nominal damping ratio

The objective function optimizes the pole placement in the left half of the s plane and maximizes the damping ratios.

Table 2. Eigen values and percentage participation of state variables - Existing method

Mode No.	Eigen value	Frequency	Damping ratio	Percentage participation of State variables
1,2	-53.3932 ± 1202.8844i	191.45	0.04	i_{c1}^{q} - 48.13 M_{ac1} - 4.00 v_{c1}^{q} - 47.81
3,4	-7.8084 ± 1692.8491i	269.43	0	i_{c2}^{q} - 47.47 N_{q2} - 3.23 M_{q2} - 2.12 v_{c2}^{q} - 47.17
5	-742.7430 + 0i	0	1	v_{dc1} - 25.59 i_{dc1} - 74.27

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6	-241.9350 + 0i	0	1	v_{dc1} - 72.23 i_{12}- 3.36 i_{dc1} - 24.14
7,8	-92.5183 ± 57.3518i	9.13	0.85	i_{c1}^{d} - 29.29 v_{s1}^{d} - 24.99 v_{c1}^{d}- 45.17
9	-101.0766 + 0i	0	1	i_{c1}^{d} - 1.53 i_{c1}^{q} - 1.01 v_{s1}^{d} - 1.24 v_{c1}^{d} - 3.60 M_{ac1} - 91.60 v_{c1}^{q} - 1.01
10	-20.9714 + 0i	0	1	i_{c1}^{d} - 19.43 v_{s1}^{d} - 6.42 v_{c1}^{d} - 69.59 N_{ac1} - 3.81
11,12	-102.1331 ± 53.0863i	8.45	0.89	i_{c2}^{d} - 26.81 v_{s2}^{d} - 25.33 v_{c2}^{d} - 46.64
13	-113.0152 + 0i	0	1	i_{c2}^{d} - 6.77 v_{s2}^{d} - 6.34 v_{c2}^{d} - 17.81 N_{q2} - 65.64 M_{q2} - 1.47
14	-1.3914 + 0i	0	1	v_{s1}^{d} - 1.23 v_{c1}^{d} - 6.51 N_{ac1} - 92.09
15,16	-41.1891 ± 53.3157i	8.49	0.61	v_{dc1} - 5.08 v_{dc2} - 44.92 i_{12} - 48.94 i_{dc1} - 1.06
17	-75.0768 + 0i	0	1	v_{c2}^{d} - 1.18 N_{q2} - 2.20 M_{q2} - 94.26
18,19	-3.3118 ± 6.3977i	1.02	0.46	i_{c2}^{d} - 4.95 M_{p2} - 5.39

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				v_{c2}^{d} - 44.15 H_{q2} - 44.44
20	-0.0001 + 0i	0	1	M_{dc1} - 99.97
21	-0.0224 + 0i	0	1	N_{dc1} - 99.98
22	-2.6227 e-08 + 0i	0	1	N_{p2} - 5.70 M_{p2} - 5.68 H_{q2} - 88.62
23	-3.8159 e-07 + 0i	0	1	N_{p2} - 32.68 M_{p2} - 32.54 H_{q2} - 34.78

Table 2 lists the eigen values and their corresponding frequencies and damping ratios of the system obtained using the existing tuning method.

3.3. Small signal stability-based tuning for LVRT enhancement

The proposed tuning methodology is formulated to provide LVRT support and reduce DC voltage oscillations, in addition to the traditional control objective. The problem is formulated as a minimization problem which will search for the best pole position within the search space.

$$Objectivefunction = min \sum_{i=1}^{m} \{W_{smi} * (\sigma_i - \sigma_0)^2\} + min \sum_{i=1}^{m} \{W_{dmi} * (\zeta_0 - \zeta_i)^2\} \quad (38)$$

where, $W_{smi} = p_{\sigma_i}/\sigma_i$, weighing factor assigned to the LVRT sensitive modes

$W_{smi} = 1/\sigma_i$, weighing factor assigned to the non-LVRT sensitive modes

p_{σ_i} - sum of participation of the 6 state variables pertaining to MRPC in ith mode, if the sum of participation of LVRT state variables is 40 %, then p_{σ_i}=40

$W_{dmi} = p_{\zeta_i}/\zeta_i$, weighing factor assigned to the damping of DC voltage sensitive modes

$W_{dmi} = 1/\zeta_i$, weighing factor assigned to the damping of non-DC voltage sensitive modes

p_{ζ_i} - sum of participation of the 6 state variables pertaining to DVC in ith mode

The objective of the optimization procedure is to arrive at an ideal tradeoff between optimizing the LVRT sensitive modes, simultaneously minimizing the destabilizing effect of tuning on other modes. The emphasis on the LVRT sensitive modes and DC voltage modes is ensured by assigning appropriate weighing factors.

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Table 3. Eigen values and percentage participation of state variables - Proposed method

Mode No.	Eigen value	Frequency	Damping ratio	Percentage participation of State variables
1,2	-53.4506 ± 1202.6422i	191.41	0.04	i_{c1}^{q} - 48.11 M_{ac1} - 4.00 v_{c1}^{q} - 47.79
3,4	-38.6655 ± 741.6097i	118.03	0.05	i_{c2}^{q} - 46.49 N_{q2} - 3.41 M_{q2} - 4.59 v_{c2}^{q} - 45.47
5	-608.2850 + 0i	0	1	v_{dc1} - 29.44 N_{dc1} - 1.27 i_{dc1} - 69.06
6	-210.3407 + 0i	0	1	v_{dc1} - 64.59 i_{12} - 3.84 N_{dc1} - 9.25 i_{dc1} - 21.87
7	-103.8532 + 0i	0	1	i_{c1}^{d} - 15.31 i_{c1}^{q} - 1.06 v_{s1}^{d} - 13.13 v_{c1}^{d} - 36.76 M_{ac1} - 32.33 v_{c1}^{q} - 1.35
8,9	-61.2389 ± 44.5748i	7.09	0.81	i_{c1}^{d}- 29.96 v_{s1}^{d} - 25.87 v_{c1}^{d} - 43.21
10	-81.0292 + 0i	0	1	i_{c1}^{d} - 25.14 v_{s1}^{d} - 21.00 v_{c1}^{d} - 51.30 M_{ac1} - 1.52
11,12	-100.5926 ± 55.6933i	8.86	0.87	i_{c2}^{d} - 27.50 v_{s2}^{d} - 25.71 v_{c2}^{d} - 45.97
13,14	-47.3088 ± 50.6141i	8.06	0.68	v_{dc1} - 9.97 v_{dc2} - 39.97 i_{12} - 37.58

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				N_{dc1} - 10.52 i_{dc1} - 1.96
15	-77.6654 + 0i	0	1	i_{c2}^{d} - 1.24 i_{c2}^{q} - 5.14 v_{s2}^{d} - 1.11 v_{c2}^{d} - 2.48 N_{q2} - 9.76 M_{q2} - 77.23 v_{c2}^{q} - 2.95
16	-50.9059 + 0i	0	1	i_{c2}^{d} - 4.57 i_{c2}^{q} - 2.55 v_{s2}^{d} - 3.99 v_{c2}^{d} - 9.45 N_{q2} - 70.69 M_{q2} - 7.13
17	-0.7340 + 0i	0	1	M_{dc1} - 1.36 v_{c1}^{d} - 1.91 N_{ac1} - 96.56
18	-23.4007 + 0i	0	1	v_{dc1} - 8.44 v_{dc2} - 11.24 i_{12} - 4.11 N_{dc1} - 76.07
19	-0.0031 + 0i	0	1	M_{dc1} - 98.43 N_{ac1} - 1.54
20,21	-3.7555 ± 6.1055i	0.97	0.52	i_{c2}^{d} - 4.59 v_{s2}^{d} - 5.26 M_{p2} - 9.13 v_{c2}^{d} - 41.25 H_{q2} - 38.98
22	-6.8029 e-09 + 0i	0	1	N_{p2} - 1.87 M_{p2} - 1.74 H_{q2} - 96.39
23	-3.4464 e-07 + 0i	0	1	N_{p2} - 34.63 M_{p2} - 32.34 H_{q2} - 33.03

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Table 3 lists the eigen values and their corresponding frequencies and damping ratios of the system obtained using the proposed tuning method.

Table 4. Values of the Gain parameters obtained from Existing and Proposed Tuning method

Gain parameter	Initial value	Existing method	Proposed method
kp_{dc1}	0.1	3.048	3.048
ki_{dc1}	0.01	0.0842	76.1922
kp_{fd1}	0.01	0.0083	0.005
ki_{fd1}	0.0001	0.0001	0.0053
kp_{ac1}	5	37.75	69.9
ki_{ac1}	50	50	50
kp_{fq1}	10	10	10
ki_{fq1}	1000	1000	1000
kp_{p2}	0.5	0.0224	0.19
ki_{p2}	0.05	2.0319 e-06	1.0098 e-06
kp_{fd2}	0.05	0.0005	0.0017
ki_{fd2}	0.0005	0.0758	0.1298
kp_{hq2}	12	12	12
ki_{hq2}	100	96	89
kp_{q2}	8	4.24	6.08
ki_{q2}	80	604.8	385.44
kp_{fq2}	4	3.76	0.546
ki_{fq2}	40	284.4	40
T_{dc}	0.001	0.001	0.0011
T	0.005	0.005	0.005

Table 4 lists the difference between values of the gain parameters for existing tuning method and proposed tuning method. From Fig. 1, it can be seen that $kp_{hq2}, ki_{hq2}, kp_{q2}, ki_{q2}, kp_{fq2}$, ki_{fq2} are the gain parameters of the MRPC loop and $kp_{dc1}, ki_{dc1}, kp_{fd1}, ki_{fd1}$ are the gains corresponding to the DC voltage controller. The optimization technique focuses on providing optimal LVRT support and reduce DC link voltage oscillations by prioritizing the state variables and gain parameters associated with it. The system is tuned at steady state, and the same gain parameter values are used to get better performance during the occurrence of fault or low voltage pocket. Overall stability of all the modes is ensured for various initial operating

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conditions. Best choice of W_{smi} and W_{dmi} is the optimal solution ensuring maximum LVRT support, minimum DC bus voltage ripple and least steady state error in reference tracking of voltages and powers.

4. Results and Discussions

In this paper, the system is modeled as a two terminal VSC-HVDC, where the AC systems on both sides of the VSC-HVDC link are replaced by their thevenized equivalent voltage and impedance. From Fig. 1, Converter 1 acts as the Slack converter and controls DC Link Voltage and AC Bus voltage. Converter 2 controls the Real and Reactive power transferred between the AC and DC systems. Table 5 gives the reference set point values for the controllers, system and DC cable data. The system is modeled and simulated in PSCAD/EMTDC. The fault is designed as a timed fault logic with defined fault impedance between Converter 2 and grid from time 1.5 s to 2 s.

Table 5. Reference set point values, System Parameters and DC Cable Parameters

Reference variable	**Reference value**
$V_{dc1-ref}$	400 kV
V_{s1-ref}	1.0 pu (230 kV)
P_{2-ref}	100 MW
Q_{2-ref}	70 MVAr
System Parameters	**Value**
Rated Power, P_{rated}	2000 MVA
AC Bus voltage, V_s	230 kV
DC Link voltage, V_{dc}	400 kV
DC Capacitance, C_{dc}	300 µF
Frequency, f	50 Hz
DC Cable Parameters	
Length	200 km
Resistance	0.07 (Ω/km)
Inductance	5.97 (mH/km)
Capacitance	0.13 (µF/km)

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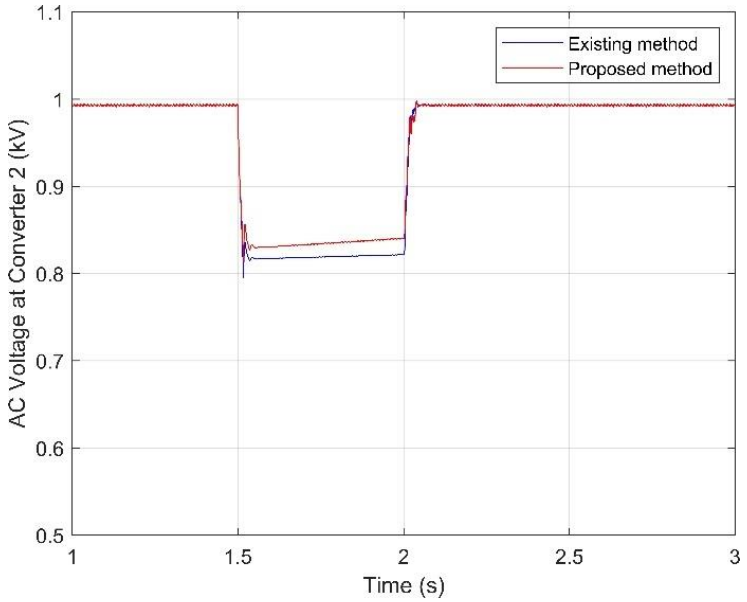

Fig. 2. Grid Voltage at Converter 2

Fig. 2 shows the voltage at the PCC of the converter 2 for MRPC with both existing and proposed tuning method for a fault impedance of 30 Ω. The PCC voltage with the proposed tuning methodology is healthier than the PCC voltage with existing tuning methodology.

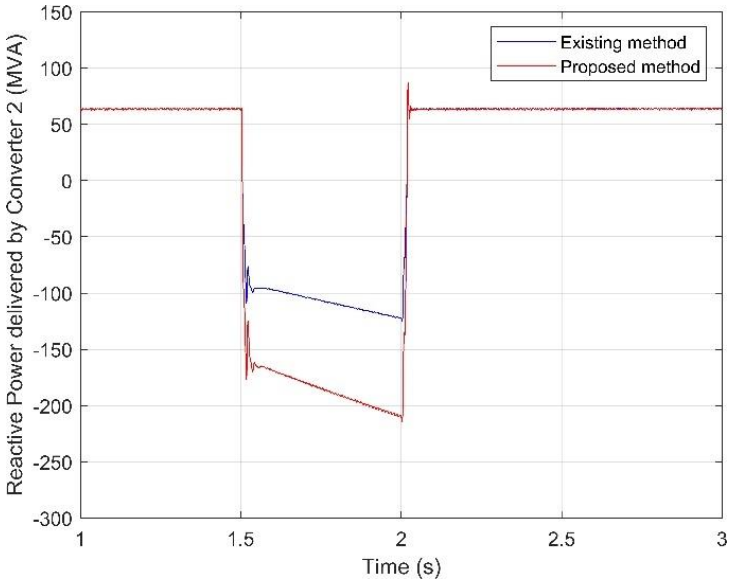

Fig. 3. Reactive Power delivered by the converter 2

Fig. 3 shows the reactive power delivered by the converter 2. It can be observed that the converter tries to provide maximum reactive power support in case of proposed tuning than existing tuning method.

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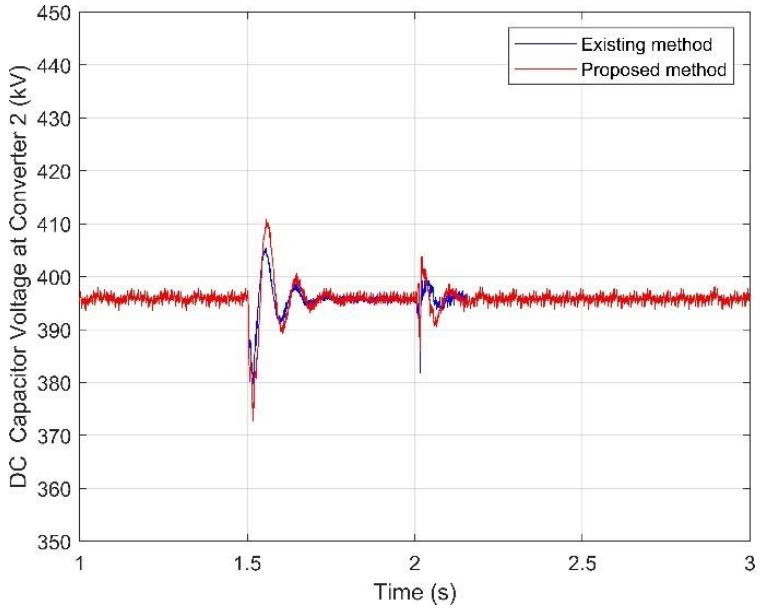

Fig. 4. DC Capacitor voltage at Converter 2

Fig. 4 shows that proposed tuning also contributes to mitigating DC voltage oscillations at converter 2 where DC link voltage controller is absent. The power balance equations of the AC/ DC interactions are fully represented. The current $i_{c1\_ref}^{d}$, of the slack bus converter is computed algebraically using i_{dc1_ref}. This ensures needful DC voltage balancing during ride through period, simultaneously maximizing LVRT support capability.

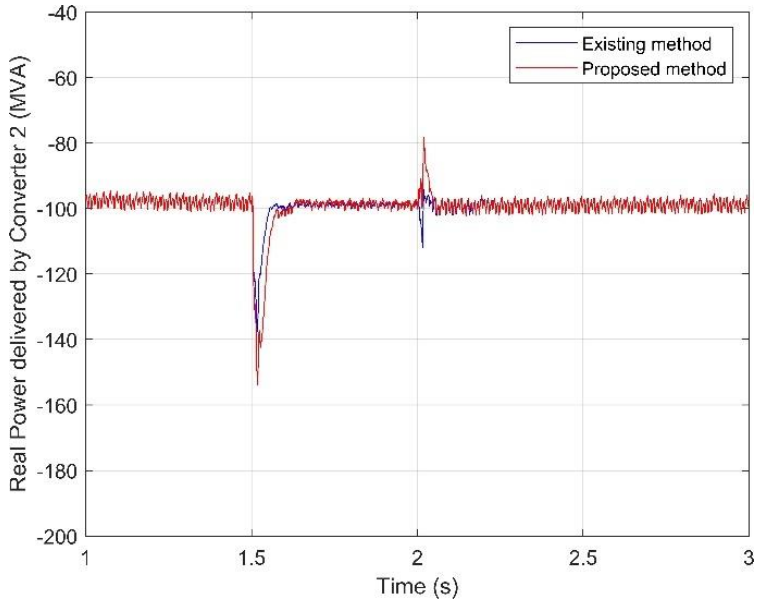

Fig. 5. Real Power delivered by the converter 2

Fig. 5 shows the real power transferred between the AC and the DC system of the converter 2.

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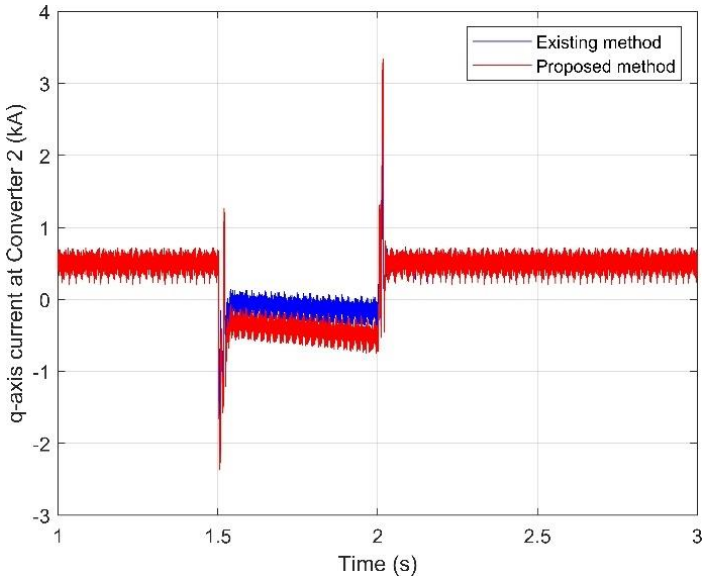

Fig. 6. q-axis current of converter 2

Fig. 6 show the q-axis current of converter 2. The limits for the currents during fault can be expressed as $\left[i^{q}_{c2\_ref\_fault}\right]^{i_{c2\_max}}_{i^{q}_{c2\_ref}}$ and $\left[i^{d}_{c2\_ref\_fault}\right]^{i^{d}_{c2\_ref}}_{0}$. The proposed controller ensures satisfactory ride through characteristics without controller mode switching. It can be observed that by optimizing the reactive power transmitted between the AC and DC systems, the converter can provide better LVRT support.

During steady state conditions, the functioning of the MRPC is same as the conventional RPC. A difference in the operation of the two types of controllers arise only when a disturbance or a fault occurs. During fault, following the voltage dip, the modulating signal from the outermost AC voltage control loop becomes non zero. The Q_{2_ref} signal is thus modulated to provide reactive power support and improve the voltage profile satisfactorily. From the results presented, tuning of controllers using linearized state space analysis yield improved time domain performance.

5. Conclusion

In this paper, an optimization-based tuning technique is proposed for a 2-Terminal VSC-HVDC system with a Modified Reactive Power Controller (MRPC), which prioritizes LVRT-sensitive modes. The proposed controller is designed to provide enhanced LVRT support without requiring controller mode switching operations or dynamic gain tuning. The dynamic equations of the two-terminal HVDC link are perturbed and linearized across a range of steady-state operating points. Various modes of the system are identified, and the participation of state variables in LVRT-sensitive and DC voltage-sensitive modes is examined. Sequentially, the controller parameters are tuned starting from the most critical mode to the less critical ones.

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The overall stability margin of the system is enhanced significantly. The proposed tuning method demonstrates superior performance across various initial operating conditions and types of faults. The coupling between DC voltage and AC power is thoroughly addressed in the design of the slack converter. Validation of the optimization-based controller tuning algorithm is achieved through time-domain simulations. Compared to existing methods, the MRPC with the proposed tuning provides enhanced reactive power support, optimizing LVRT capability during various types of voltage dips. The oscillations in the DC bus voltage and the real power transmitted between the AC and DC systems are reduced through coordinated control of the sending-end and receiving-end converters. The system has been simulated in PSCAD, demonstrating that the MRPC with the proposed tuning methodology functions effectively under normal operating conditions and during Low Voltage Ride Through (LVRT) situations.

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