Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

Performance Analysis of a Novel Multilevel Inverter with Reduced Number of Switches

Renukaprasad .G, V. S. Kirthika Devi
Department of Electrical and Electronics Engineering, Amrita School of Engineering, Bangalore, Amrita Vishwa Vidyapeetham, India
renukaprasad25@gmail.com, S_kirthika@blr.amrita.edu

Abstract—Multilevel inverters (MLI) are important and widely accepted under DC to AC converter family for medium and low power applications. In the paper a "new inverter topology" for multi-level is developed. The primary purpose of the work is to reduce the switch count number for considerable level of output voltage and also to reduce gate drives required. It also aims at analysis of performance of proposed topology of new multilevel inverter. Output of fifteen stages is generated from the proposed topology. For which only eight switching devices, four diode and three asymmetrical sources are used. Thus, the space and cost for installation is reduced. The designed topology is simulated with normal "pulse width modulation (PWM)" as well as "sinusoidal pulse width modulation (SPWM)". Both the Simulation results are discussed with respect to "output voltage, current, Total Harmonic Distortion (THD)". A comparative study is also made between the topology developed with few other latest MLI topologies.

Index Terms—H bridge multi-level inverter, IGBT, Total Harmonic Distortion, Asymmetrical MLI.

I. INTRODUCTION

Renewable energy is an alternative source to meet increasing load demand. Multilevel Inverters are the major component in renewable energy applications [1]. The demand for medium and high voltage inverters has been rising in the recent years. Over the past decade multilevel inverter topologies have gained more popularity. The Fig.1 shows a block diagram in which multilevel inverter along with renewable energy generation system is represented. In which renewable sources like solar, wind, tide and many more energy sources are integrated and they are connected to converter which can be a boost converter. The DC power from the converter is then stored in a battery. DC power from the battery is then converted to AC power which is required for almost all loads. Inverter are the one which is required for this conversion. We normally look for inverter which gives more number of voltage level to improve the quality of output which results in multilevel inverter. Diode clamped, Cascade H-bridge and Capacitor clamped are the basic "conventional multilevel inverter topologies". Among those Cascade H-bridge is the most simple one with respect its structure and complexity. This can easily employed in renewable energy system such as Solar, Wind, Tidal ettc [2]-[4]. All electrical field like High Voltage Direct Current (HVDC), Renewables Energy Systems (RES), Distributed Generation Systems (DGS) etc. finds the application of MLI.

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

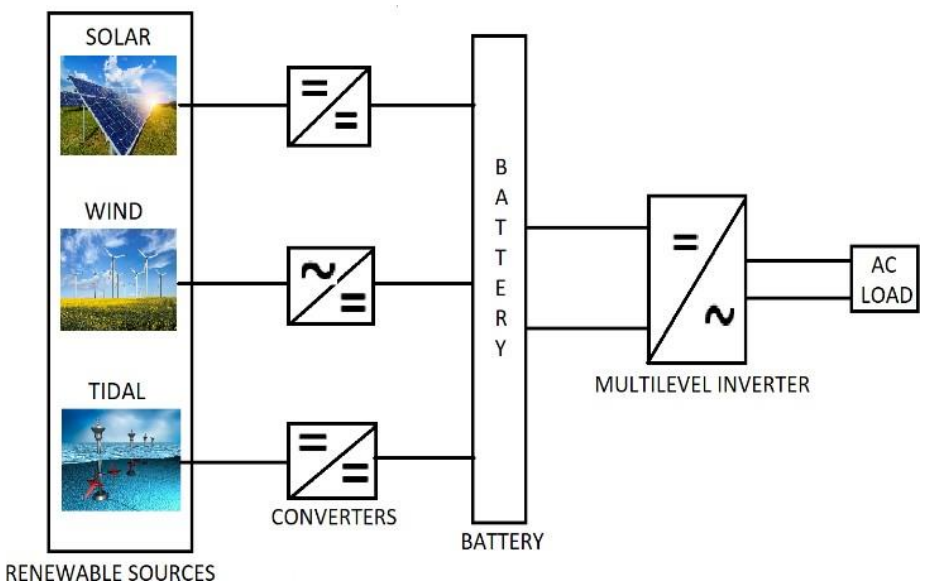


Fig.1 Block diagram of Renewable Energy system

The "Conventional multilevel inverter topologies" face issues like large number of source requirement, large switch requirement etc [5]. Various MLI were proposed in the past decade to mitigate the issues with conventional one. Number of switches, number of voltage sources, capacitor utilized , modularity of topology etc. are the few design aspect of MLI. Primarily based on those, many new Multi-stage inverter topologies had been proposed and are provided in the literature

Voltage source magnitude selection is another challenging aspect of Multi-level inverter. Based on this aspect MLI are classified as symmetrical and asymmetrical. Symmetrical Multi-level inverter are those in which identical sources are used and Asymmetrical Multi-level inverter are those in which sources with unequal magnitude are used. In symmetrical multi-level inverter more number of switching combination is possible. This will improve the inverter performance. But the problem is that the switch count, gate driver count and dc voltage count required is more. This will increase size and cost. But in asymmetrical configuration higher levels of output for same components and sources is possible [6]-[7]. Although these conventional multilevel inverters face some issues with respect to number of switches, voltage balancing, etc. they are advantageous with reference to power quality. "Pulse width modulation" for these converters to control the output is another challenging and important aspect [8]-[9].Lot of research is going on to alleviate the issues with the multilevel inverters and have been published many papers on MLI addressing the problems.

In paper [10] basic "multilevel inverter" is discussed. This paper also respresents extension of basic unit to achieve more levels. A comparative analysis of few different topologies with the topology designed is also made. It is found that 53 voltage steps using 22 IGBTs is possible in the

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 Revised: 02-02-2024 Accepted: 07-03-2024

work proposed. It is inferred here that to obtain output with multiple stages a high number of switches are necessary. In paper [11] a new topology with five sub module is used. Both "symmetrical and asymmetrical modes" of operations are demonstrated on the topology. It is certain that the designed topology is advantages in stages of voltage generated for given quantity of switches. A new topology in asymmetrical mode with reduced switch count is detailed in paper [12]. Output voltage with 17 stages for 12 switches and 4 sources is obtained in the work. A cascaded MLI is presented in [13]. In this, to get higher levels a basic unit is connected in series. A comparative study of the topology built is also made with conventional cascaded MLI. Accordingly, it is noticed that a less number of IGBTs is sufficient comparatively.

In paper [14], a new MLI which extendable is proposed. This topology has inbuilt creation of negative voltage, here 8 switches and 3 sources are used to get a voltage level of 7 with 8 gate drive. A new MLI which is cascade switch ladder is presented in [15]. The topology can yield output voltage with a large number of steps. Here 15 level output is implemented with 10 switches, 3 sources, 10 gate drive. In [16] a staircase output voltage generation is proposed with minimum switch count and gate drives for "15 level output voltage" using 10 switches, 3 sources and 9 drives.

In this paper, work is achieved with the intention of developing "new multilevel inverter" with minimal switch count number, gate drive and source while accomplishing higher "number of levels" at the same time. This paper is organized within the following section. In section II, working of designed topology is described together with the various operating modes. In section III results of the simulation of the topology designed is presented and comparative discussion on the developed topology with few other topologies is also done. Section IV summarizes the paper.

II. PROPOSED MULTILEVEL INVERTER

A. Proposed Multilevel Inverter topology

Topology with 8 switches and 4 diodes proposed is shown in Fig.2. It consists of 8 IGBT from S1 to S8 and four diode from D1 to D4. Switches from S3 to S6 form H bridge. This H bridges is connected with remaining "switches and diodes" as shown in Fig.2 to generate 15 level output. The system proposed is operated in asymmetrical configuration.

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

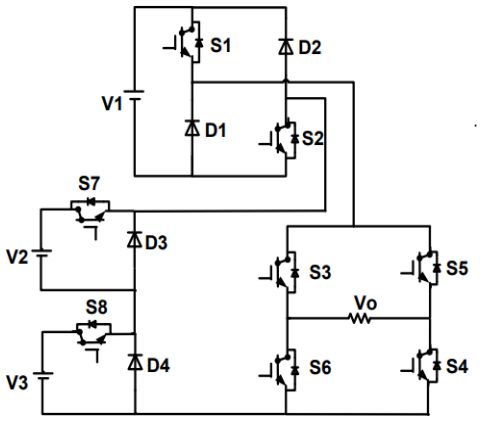
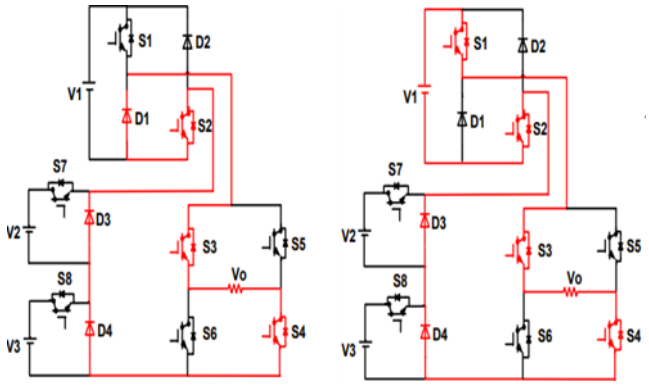


Fig.2. Proposed 15 level inverter topology

The "magnitude of voltages" V1, V2, V3 have different voltage values, i.e., V1=Vdc and V2=V3=3Vdc. The proposed network generates output voltage with 15 levels i.e., ±Vdc, ±2Vdc, ±3Vdc, ±4Vdc, ±5Vdc, ±6Vdc, ±7Vdc and zero.

B. Modes of operation.

In positive half cycle there will be modes from 0 to 7, which are shown in Figs. 3 (a)-(h). In mode 0, switches S2, S3 and S4 are conducting along with diodes D4, D3 and D1 to yield a voltage of zero at load. In mode 7, switches S1, S3, S4, S8 and S9 are conducting by which a voltage of 7 Vdc is appearing at load as shown in Fig.3(h). In the circuit shown, switches which are conducting is shown in red color and the switches which are not conducting is shown in back color. The current path can then be traced along the red path for the remaining modes of operation. Similar explanation can framed for the negative half cycle. And switching pattern for the negative half cycle topology is also illustrated in Table I.



(a) (b)

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

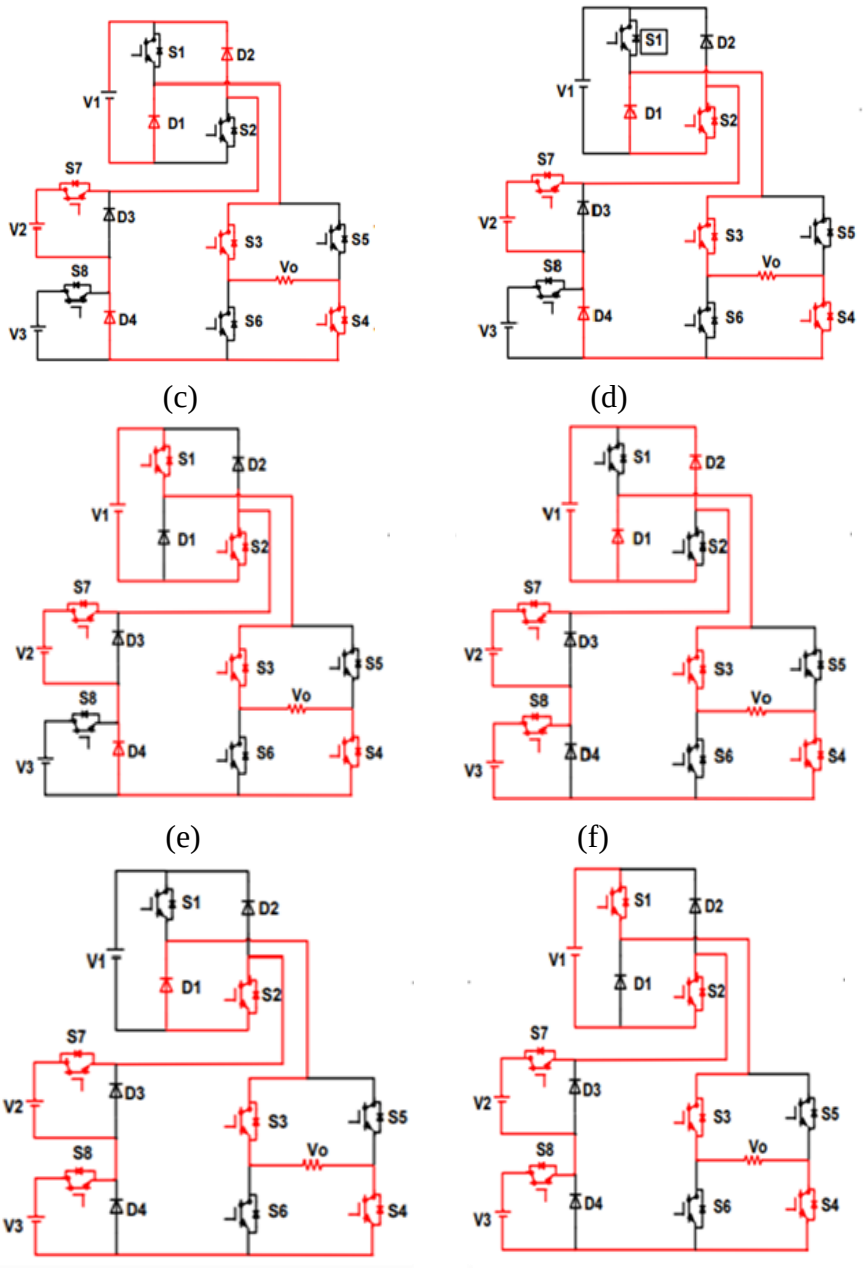


Fig. 3. Modes of operations of the proposed topology in positive half cycle.
a) Mode 0: Vo = 0. b) Mode 1: Vo = Vdc. c) Mode 2: Vo = 2Vdc. d) Mode 3: Vo = 3Vdc.
e) Mode 4:Vo = 4Vdc. f) Mode5: Vo = 5Vdc. g) Mode 6: Vo = 6Vdc. h) Mode 7: Vo = 7Vdc

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

III. SIMULATION RESULTS AND DISCUSSION.

MATLAB/SIMULINK tool is used in verification of the topology developed. The pulses for the switches are generated by means of conventional "pulse with modulation (PWM)" as well as "sinusoidal pulse width modulation(SPWM) ". Fifteen level output voltage achieved for the developed topology using conventional "pulse with modulation (PWM)" is shown in the "Fig. 4 (a)" and "Fig. 4 (b)" shows the output voltage waveform for the same output level with "sinusoidal pulse width modulation (SPWM)". Similarly output current waveform using conventional PWM method and SPWM are illustrated in "Fig. 5(a)" and "Fig. 5(b)" respectively. Here the load used in the simulation is the resistive load.

Table I. Switching pattern of the proposed topology

S1	S2	S3	S4	S5	S6	S7	S8	VO
1	1	1	1	0	0	1	1	7 Vdc
0	1	1	1	0	0	1	1	6 Vdc
0	0	1	1	0	0	1	1	5 Vdc
1	1	1	1	0	0	1	0	4 Vdc
0	1	1	1	0	0	1	0	3 Vdc
0	0	1	1	0	0	1	0	2 Vdc
1	1	1	1	0	0	0	0	1 Vdc
0	1	1	1	0	0	0	0	0 Vdc
1	1	0	0	1	1	0	0	1 Vdc
0	0	0	0	1	1	1	0	2 Vdc
0	1	0	0	1	1	1	0	3 Vdc
1	1	0	0	1	1	1	0	4 Vdc
0	0	0	0	1	1	1	1	5 Vdc
0	1	0	0	1	1	1	1	6 Vdc
0	1	0	0	1	1	1	1	7 Vdc

THD obtained for the output voltage is also shown in Fig. 6 for both the case. It is observed that THD got for output voltage is of 18.17%. "Fig. 7(a)" and "Fig. 7(b)" illustrates the THD level of the "output current" with conventional "pulse width modulation PWM" and "sinusoidal pulse width modulation SPWM" method respectively. It is noticed that THD got for output current is also of 18.17%.

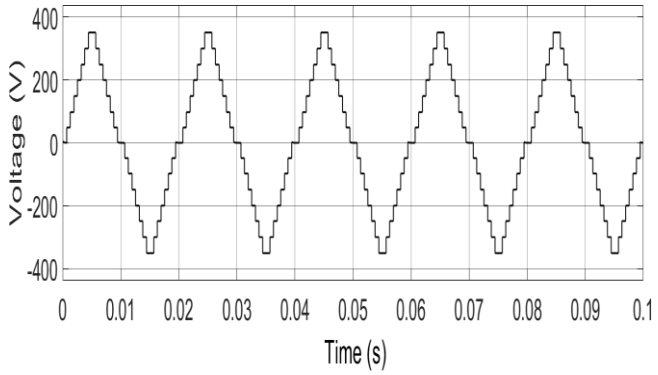
Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

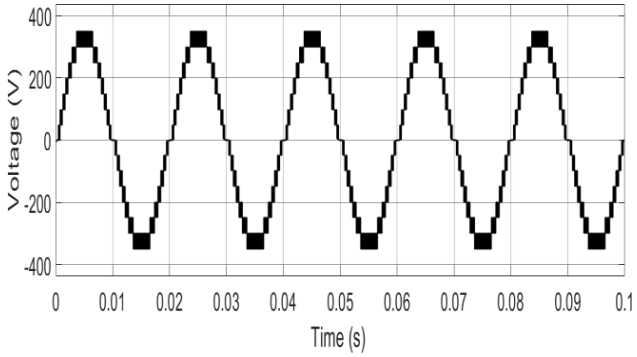
A comparative analysis is also presented in the section for the topology proposed. Three old topologies from paper [14], [15], and [16] are considered to compare with the topology designed in terms of number of switches, number of gate drives and number of source required. It is delineated in the table 2 that the MLI topology proposed generates fifteen step/level output voltage by using only 8 switches, 3 voltage sources and with only 6 gate drives as contemplate with the considered topologies.

Table 2. Quantitative delineated of the topology proposed

Topologies	Steps/Level	Sources	Switches	Gate drive
[14]	7	3	8	8
[15]	15	4	10	10
[16]	15	3	10	9
Proposed	15	3	8	6



(a)



(b)

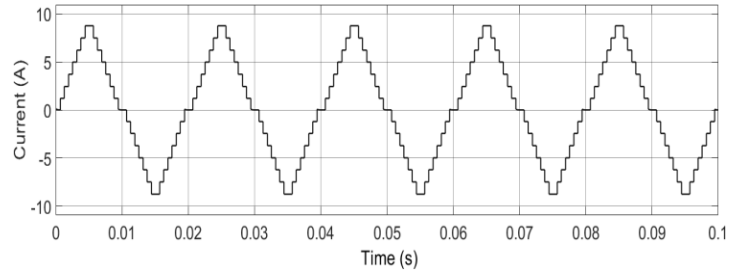
Fig. 4. (a) Output voltage waveform with conventional PWM. (b) Output voltage waveform with SPWM

Power System Technology
ISSN:1000-3673

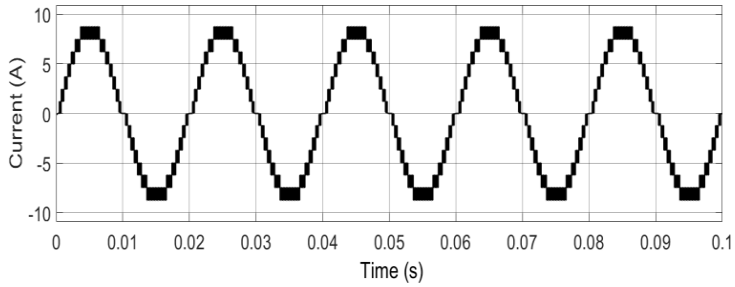
Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

IV. CONCLUSION

The paper put forward a new multi-level inverter topology with considerable minimum switch count. 15 level output with only 8 switches, 6 gate drives and 3 sources is achieved with the new topology developed. A comparative examination of the topology developed and recently published topology is also performed. Comparative analysis indicates that the simulation results are improved with a reduced number of switches, which is consistent with the topology developed.

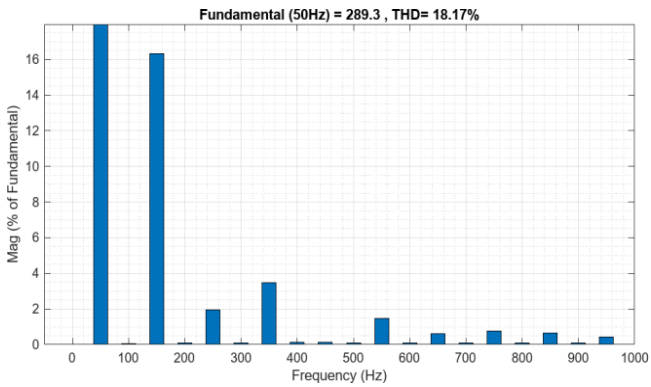


(a)



(b)

Fig. 5. (a) Output current waveform with conventional PWM. (b) Output current waveform with SPWM

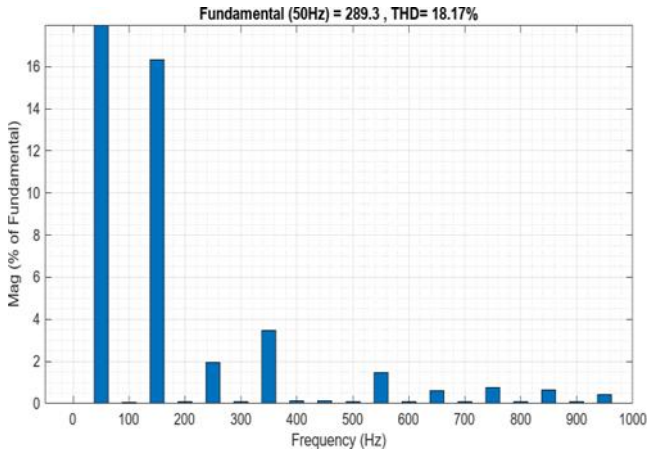


(a)

Volume 48 Issue 1 (March 2024)

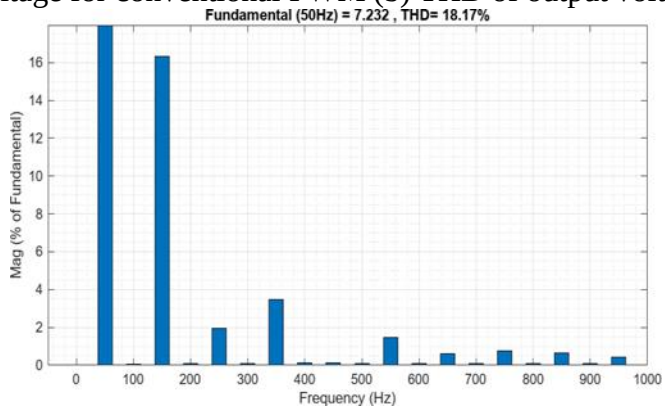
Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

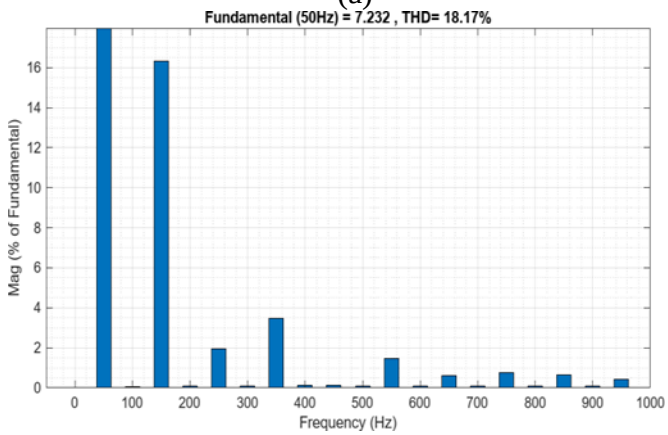


(b)

Fig. 6. (a) THD of output voltage for conventional PWM (b) THD of output voltage for SPWM



(a)



(b)

Fig. 7. (a) THD of output current for conventional PWM (b) THD of output current for SPWM

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

REFERENCES

[1]. Devi, VS Kirthika, and S. G. Srivani. "Performance assessment of PV energy conversion system with Buck-Boost and Cuk converter for cascaded H-Bridge inverter." *2016 Biennial International Conference on Power and Energy Systems: Towards Sustainable Energy (PESTSE)*. IEEE, 2016

[2]. Akagi, Hirofumi. "Multilevel converters: Fundamental circuits and systems." *Proceedings of the IEEE* 105.11 (2017): 2048-2065.

[3]. Rajkumar, R., K. Ramanathan, and M. Venkatesh Kumar. "Review On Various Multilevel Inverter Topologies For Renewable Energy Sources." *International Journal of Applied Engineering Research* 10.4 (2015): 3762-3765.

[4]. Rajkumar, R., K. Ramanathan, and M. Venkatesh Kumar. "Review On Various Multilevel Inverter Topologies For Renew.able Energy Sources." *International Journal of Applied Engineering Research* 10.4 (2015): 3762-3765.

[5]. Prabaharan, Natarajan, and Kaliannan Palanisamy. "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications." *Renewable and Sustainable Energy Reviews* 76 (2017): 1248-1282.

[6]. Venkatesha, K., and H. A. Vidya. "Analysis of Symmetrical & Asymmetrical PWM Based Single Phase AC to AC Converter for Power Quality Improvement." *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*. Vol. 5. No. 9. 2016. 7225-7232.

[7]. Devi, V S Kirthika, and Dr S G Srivani Iyengar. "A New PWM Technique For symmetric and Asymmetric Seven Level Multilevel Inverter Topology with reduced number of DC sources." *International Journal of Applied Engineering Research (IJAER), ISSN* (2015): 0973-4562.

[8]. V. S. Kirthika Devi and Srivani, S. G., "A Novel PWM Technique for Seven Level Multilevel H-Bridge Inverter Topology", *6th International Conference On Electrical Electronics Communication Robotics and Instrumentation Engineering* (Iceecie 2015). 2015

[9]. Devi, V S Kirthika, and S. G. Srivani. "Modified phase shifted PWM for cascaded H bridge multilevel inverter." *2017 Third International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)*. IEEE, 2017.

[10]. Babaei, Ebrahim. "A cascade multilevel converter topology with reduced number of switches." *IEEE Transactions on power electronics* 23.6 (2008): 2657-2664

[11]. Hosseinzadeh, Mohammad Ali, et al. "New cascaded multilevel converters based on switched-diode six-level configuration." *2017 IEEE Southern Power Electronics Conference (SPEC)*. IEEE, 2017.

[12]. Samadaei, Emad, Abdolreza Sheikholeslami, Sayyed Asghar Gholamian, and Jafar Adabi. "A square T-type (ST-type) module for asymmetrical multilevel inverters." *IEEE Transactions on power Electronics* 33, no. 2 (2017): 987-996.

[13]. Babaei, Ebrahim, Sara Laali, and Zahra Bayat. "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches." *IEEE Transactions on industrial electronics* 62, no. 2 (2014): 922-929

Power System Technology
ISSN:1000-3673

Received: 06-01-2024 *Revised: 02-02-2024* *Accepted: 07-03-2024*

[14]. Thiyagarajan, V. "New symmetric extendable type multilevel inverter topology with reduced switch count." *2019 Fifth International Conference on Electrical Energy Systems (ICEES)*. IEEE, 2019.
[15]. Alishah, Rasoul Shalchi, et al. "Optimal design of new cascaded switch-ladder multilevel inverter structure." *IEEE Transactions on Industrial Electronics* 64.3 (2016): 2072-2080.
[16]. Siddique, Marif Daula, et al. "A new multilevel inverter topology with reduce switch count." *IEEE Access* 7 (2019): 58584-58594.