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An improved KNN algorithm-based error identification for Local Binary Pattern Histogram of human emotions

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Abstract:- This research article presents the real-time implementation of an improved KNN algorithm for identifying error pixels in the Local Binary Pattern Histogram Image used for multi-face emotion recognition. The proposed method focuses on the precise identification of error pixels in the image, while the LBPH recognizes human emotions by implementing it in an FPGA device. Specifically, facial emotion recognition algorithms such as Convolutional Neural Networks (CNNs), Support Vector Machines (SVMs), and Haar cascades are used. However, the LBPH algorithm is simple, easy to implement, and highly efficient. With the inclusion of Artificial Intelligence, the LBPH can be freed from error pixels. This work utilizes a novel improved KNN algorithm to identify the error pixels added to the image. The validity of the proposed method requires error induction at random pixels of the image and verification for recognition by the improved KNN algorithm. The use of an FPGA for the proposed methods proves to be advantageous, with high throughput and low latency.

Keywords*: Multi-Face Emotion recognition, Local Binary Pattern Histogram, K-NN algorithm, FPGA, Fault Analysis.*

1. Introduction

Human facial emotions play a pivotal role in expressing an individual's behaviour, thoughts, and response to any situation. The demand for the inculcation of technology with human facial emotions derives from several applications such as marketing, healthcare, gaming, security, surveillance, computer interaction, and social robots. Though the need for human emotion identification is projected towards certain targeted services, the predominant use of mobile and portable gadgets has led to a wide range in the real world. The advent of Artificial Intelligence algorithms has effectively evolved human Face recognition; however, the face features that identify an individual are unknown to the user. This can be overcome by comparing the applied image models to identify the features of the face that accomplish the correct recognition [1]. The use of computer imaging in recognizing faces, bodies, and objects is important for socially assistive robotic applications [2]. In general, the inclusion of machine and deep learning algorithms in imaging has benefited many agricultural farms and businesses. For example, sensing crop leaves of rice and its suitability for harvesting provides accurate agribusiness and

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improves the yield cost [3]. Further, the emission tomography images of 3 × 3 Nuclear Fuel rods defects are accurately identified by the AI-based neural network algorithm [4].
Conventionally, human facial emotion recognition has been carried out using several algorithms such as Convolution Neural Networks, LSTM, Principal Component Analysis, Viola-Jones algorithms, etc. However, the Local Binary Pattern Histogram algorithm is more suitable due to its easy computation, high efficiency, and being unaffected by visible light variations. The LBPH algorithm has higher accuracy than the deep learning neural network algorithm for facial recognition in real time [5]. The LBPH descriptors are useful for a facial recognition system implemented with a low-cost embedded processor, such as an FPGA, as it merits portability and autonomy [6]. The LBPH algorithm-based two-wheel mobile robot recognizes the person and transmits an alert message to the administrator to cover the blind spots of the CCTV surveillance at data centres with high accuracy [7].

The other major issue in all imaging algorithms is the inclusion of additive error pixels in the image during the process. The identification of additive error pixels is possible by making use of machine learning and deep learning algorithms. Among all machine learning algorithms, the most versatile algorithm is the K-nearest neighbor (KNN) algorithm. The KNN algorithm is fast in identifying the faults and consumes minimal time in its computation to indicate the root variable of the fault occurrence [8]. The KNN algorithm is significant when utilized in high-dimensional spaces and complex datasets [9]. The Multi-KNN algorithm can be combined with the Speeded Up Robust Features and Backward Propagation Neural network to precisely discriminate the original face of an individual from that of the plastic surgery face of the same individual [10]. The facial recognition based on the KNN algorithm is used to avoid any proxy attendance in the bank ATM installations [11].

The challenge of human facial emotions recognition methods is the real-time implementation. Among all digital controllers, the FPGA device is meritorious with high performance, adaptability, less delay, and high throughput. The multi-toning algorithm for the removal of blue error stacked error is 30 times faster when implemented in the Zynq FPGA device [12]. The high-speed image enhancement for low-visibility videos under hazy conditions is achieved by the use of the Cyclone V FPGA device [13]. The FPGA exhibits high accuracy and rapid computing speed in implementing a contactless heartbeat monitoring system [14]. The investigation of sodium level in human calf skin through imaging is attained using the FPGA device [15]. The detection and matching of key point images with high-resolution images with an FPGA offer merits such as low power, complex manipulations, and optimized hardware [16]. The real-time FPGA-based image processing is combined with the real-time kinematic GPS to collect data with geo-tags to monitor the crops. The fusion of FPGA with the GPS enables overcoming design complexity, high computation cost, limited accuracy in GPS, and

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low resolution of images [17]. The challenge of low visible light in real applications is overcome by making an FPGA implemented Retinex algorithm that exhibits low power and minimum device utilization [18]. The CNN algorithm, when implemented in an FPGA device, can attain high power efficiency with low latency and high throughput, as FPGA devices are parallel in their computing and thus make them suitable for real-time object identification systems [19].

In this work, the grey-scale image of multi-face emotions is identified for induced additive error pixels in the LBPH image using an improved KNN algorithm and verified with the FPGA device for real-time implementation. The LBPH algorithm is implemented in an FPGA with a resolution of 48 X 48 image pixels. Then the error pixels are randomly induced into the LBPH-derived image pixel. The induced error pixel is identified by the FPGA-based improved KNN algorithm. The next section details the proposed fault identification of the error pixel of the LBPH image using the improved KNN algorithm. Section III indicates the verification of the proposed method in real-time using the Artix 7 FPGA board and discusses the validation of the proposed method by utilizing the Kaggle dataset. Section IV concludes with the merit of the proposed method.

2. The Proposed Method: Error Pixel Identification in LBPH image using Improved KNN Algorithm

The proposed method analyses the error pixel of the LBPH image using the improved KNN algorithm to identify the emotion of the multi-face images. The multi-face human emotions considered for identification are anger, contempt, disgust, fear, happiness, sad, and surprise. In this work, the error is randomly induced at the interim stage of the LBPH process. The design flow of the proposed methods can be divided into three sections, namely i) Design flow of LBPH for grey-scale image to identify multi-face emotions, ii) Design flow for the improved KNN algorithm for error analysis in LBPH image, and iii) HDL design flow for the FPGA implementation. Figure 1 shows the overall design flow for the proposed method to analyze the induced error pixel using the improved KNN algorithm.

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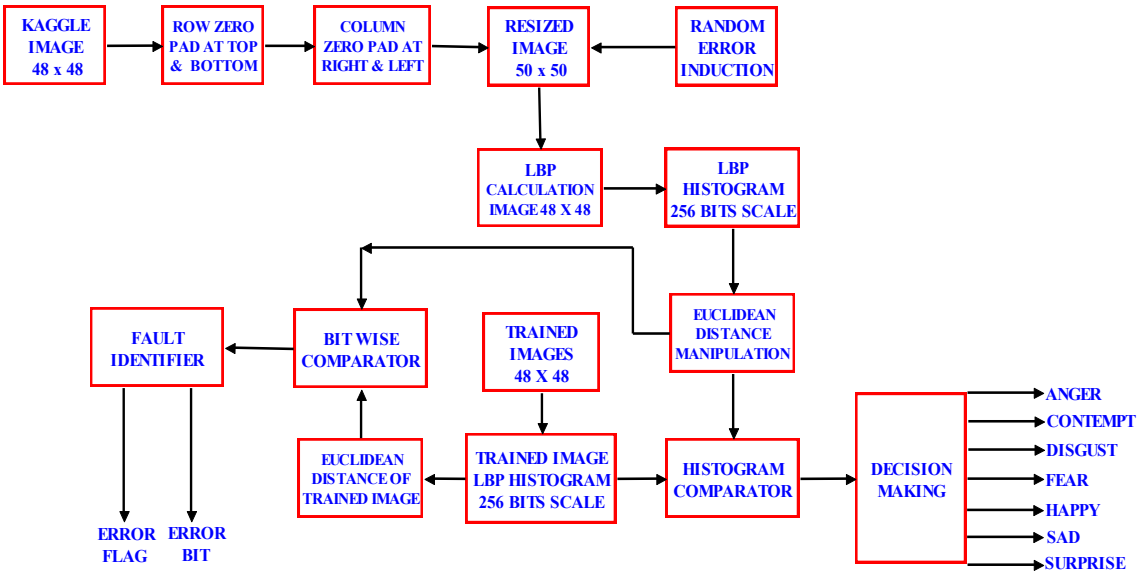

Figure 1. Block diagram of the proposed error pixel identification in LBPH multi-face human image

A. Design flow of LBPH for grey-scale images to identify multi-face emotions

The LBPH image is attained by performing a series of operations on the considered image. The image datasets are taken from the KAGGLE database with a resolution of 48 × 48 pixels. The pattern of 48 × 48 grey-scale multi-face images with the intensity resolution of 8 bits is given in Figure 2. There are 48 rows and 48 columns in the image represented as Row_1-Row_{48} and C_1-C_{48}, respectively. To evaluate the LBPH of the given 48 rows and 48 columns, the top and bottom rows with the rightmost and the leftmost columns are to be zero-padded. This inclusion of the zero pads increases the resolution of the image to 50 × 50 pixels. These 50 × 50 zero-padded images are utilized for the derivation of the LBPH image with a resolution of 48 × 48 pixels; otherwise, the image resolution of the LBPH image will be reduced to 47 × 47 pixels. This will lead to the loss of pixels of the input image. Figure 3 gives the zero pad images with the top and bottom rows with zero values, the rightmost and leftmost columns are assigned zero values to form a 50 × 50 image pixel.

For the sake of LBPH manipulations, the 50 × 50 image is split into 3 rows, starting from Row_1 to Row_{50} as LBPH Row1 from Row_1-Row_3, LBPH Row_2 from Row_2-Row_4, and for the last LBPH Row_{48} is derived from Row_{48}-Row_{50}. Each of the pixel values of the LBPH rows is derived from the 3 × 3 pixels of the 50 × 50 zero-padded image. Figure 4 depicts the procedural diagram for the LBPH manipulation from the 50 × 50 zero pad image. The sample of 4 rows is presented to elaborate on the LBPH manipulation in the first and second row. The LBPH pixel L_{11} requires the Row_1-Row_3 and $Column_1$-$Column_3$ values to be considered as 3 × 3 images.

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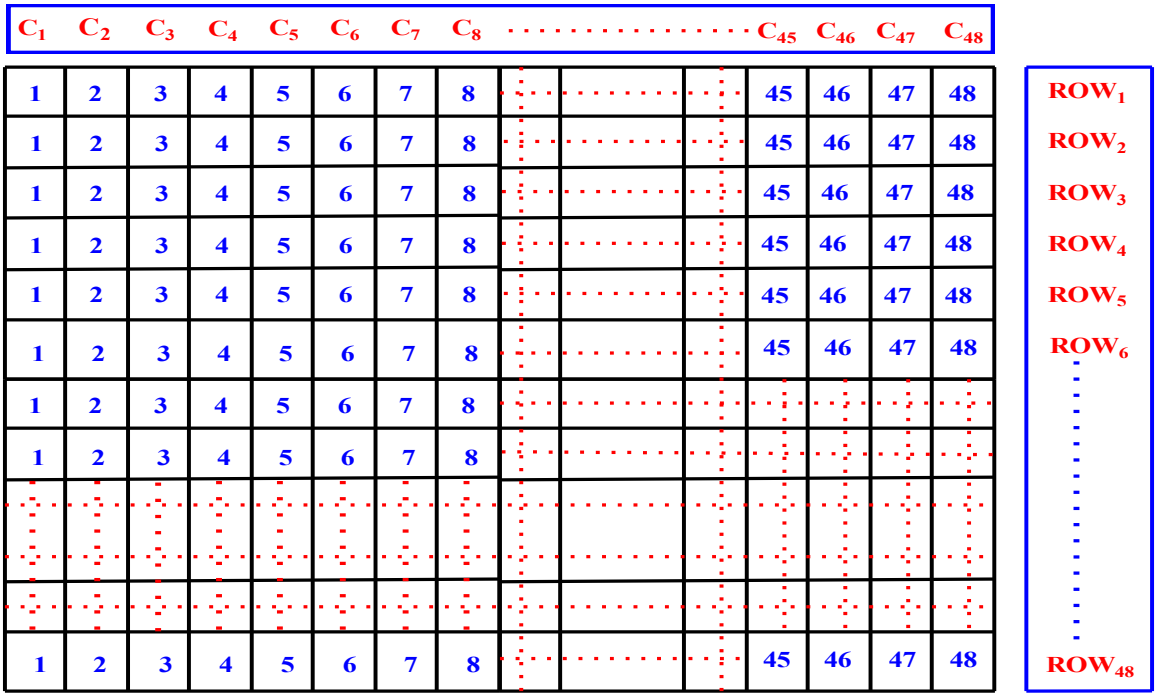

Figure 2 Resolution for the 48 × 48 Image considered for LBPH algorithm

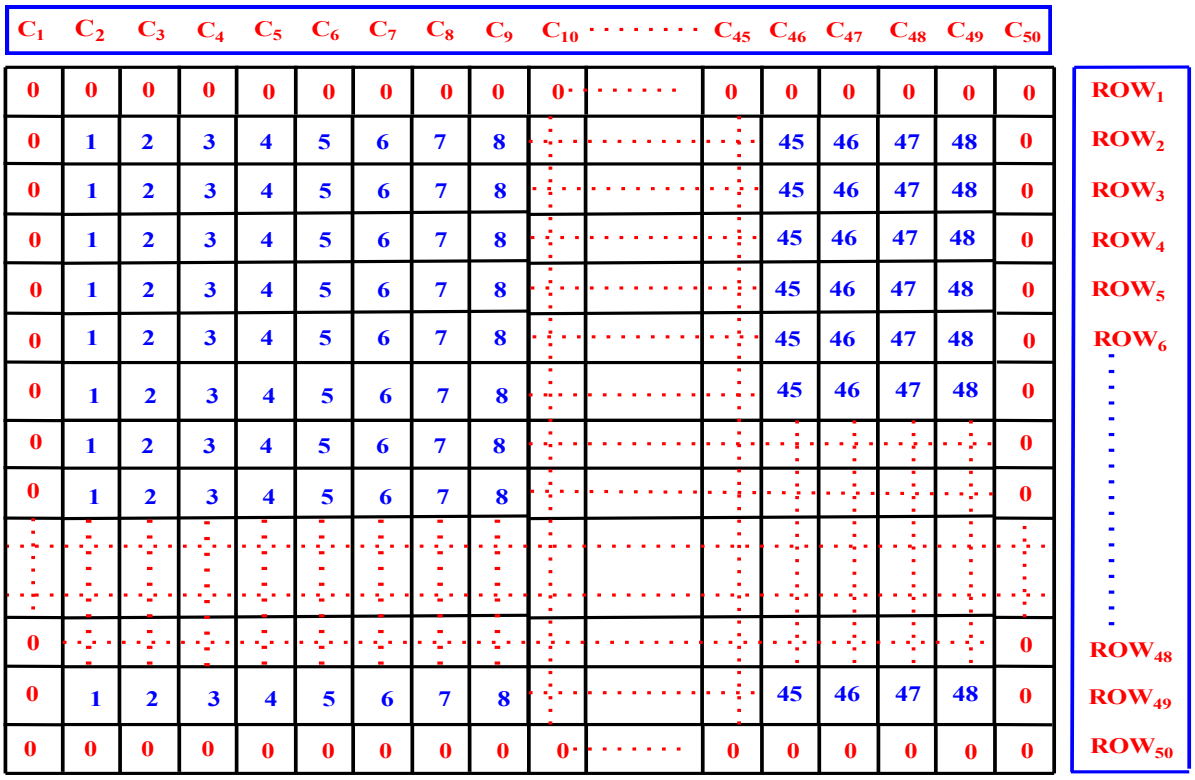

Figure 3 Zero pad of rows and columns for the 48 × 48 image in the LBPH algorithm

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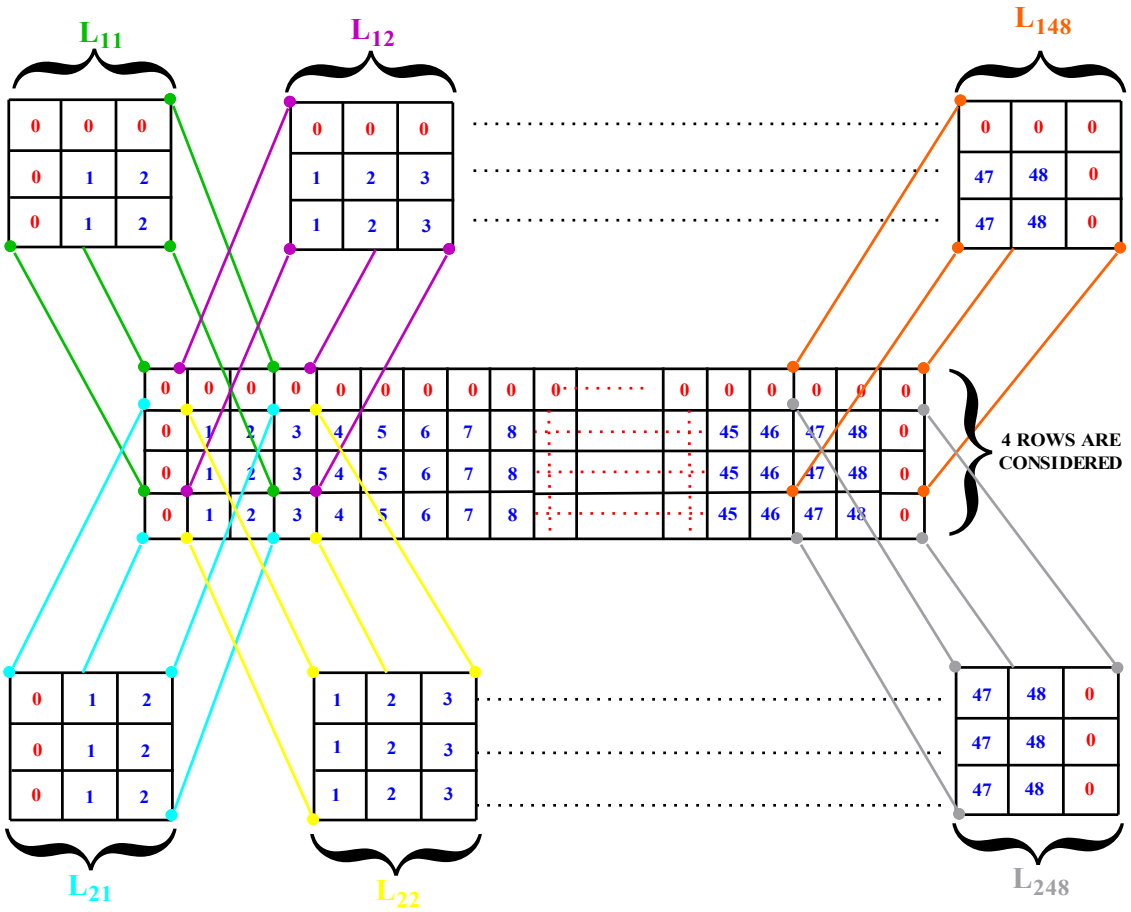

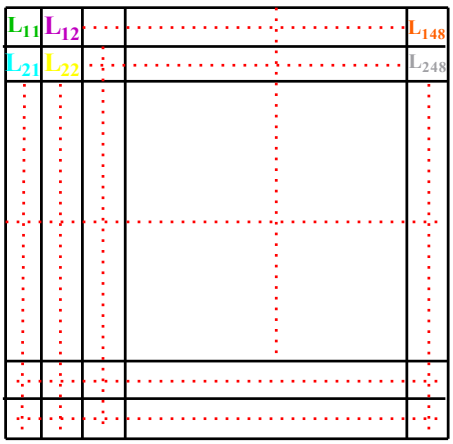

Figure 4 LBPH operation for the samples Rows of 1 to 4

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I_0	I_1	I_2
I_7	I_C	I_3
I_6	I_5	I_4

Figure 5 LBPH representation of 3 × 3 matrix with centre pixel and neighbour pixels

Over this 3 × 3 image, the LBPH manipulation is applied by considering the centre pixel as I_C and the remaining pixels as I_0 to I_7, as shown in Figure 5. Now the values of I_0 to I_7 are subjected to the formula as given in (1) to evaluate the values as S(0) to S(7).

$$LBPH = \sum_{N=0}^{7} S(I_N - I_C)2^N \quad (1)$$

$$S(Z) = \begin{cases} 1, Z \geq 0; \\ 0, Z < 0; \end{cases} \quad (2)$$

These evaluated S values are checked as per the condition given in (2); if the S value is less than 0, it is considered as a binary value of '0', and if the evaluated S value is greater than or equal to 0, it is considered as a binary value of '1'. All S values are assigned the same conditional check. Now these binary values are concatenated to form the 8-bit value equivalent for the pixel. The orientation of the binary values is S(0) as the MSB and S(7) as the LSB. For the sake of clarification, the L11 is the evaluation of the first pixel in the LBPH image. To attain the LBPH value, the 3 × 3 matrix is considered and evaluated as per the LBPH formula and conditionally checked for the derivation of the 8-bit binary values. The same process is continued till the end of the last pixel for the 48 × 48 LBPH image. The process is complex when implemented in the logic of an FPGA hardware device, as it has to calculate for all 2304 pixels of the LBPH image.

The objective of the proposed work is to identify the error pixels of the LBPH image. To validate this objective, the random error is induced into the image pixel at the zero pad stage of the LBPH process. This induction of error pixels will verify the correctness of the proposed improved KNN algorithm. The induction of the error that is added with the resolution of 50 × 50 zero pad images is identified in the 48 × 48 LBPH image. The process involved in the identification of error pixels consists of the comparison of the trained image samples and the

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test image. The next section details the algorithm for the improved KNN in indicating the error pixel.

B. The Improved KNN Algorithm for Error Pixel Diagnosis

The proposed method involves the improved KNN algorithm to identify the induced error pixel in the LBPH image. The 48 × 48 LBPH grey-scale image consists of 2304 pixels, and each pixel is equipped with an intensity of an 8-bit representation. The grey-scale LBPH image with a resolution of 8 bits constitutes a total bit count of 18432 bits. These 18432 bits are taken in serial through the Parallel In Serial Out (PISO) register for both the test image and trained image. The serial values of 18432 bits are logically XORed for the test and trained images. The serial bits from the resultant XOR operations are accumulated as 18432 image bit values by using a Serial In Parallel Out (SIPO) register. The test image is logically XORed with 7 trained images to determine the closest match. The 18432 image bits from the XOR operation with all 7 trained images are sorted to identify the minimum 18432-bit value. Then the conditional checker scans through all the 18432 bits and compares them with the trained sample bit to identify the error-induced pixel. When the error is identified, the error flag is set to the "ON" state, else to the "OFF" state. The corresponding pixel bits position is evaluated with the counter clock circuit and indicated with a resolution of 2^{15} bits to accommodate the 18432 value. The improved KNN algorithm does not use any distance calculation to evaluate the nearest image to the trained sample image. Also, the identification of image matching is achieved by the simple utilization of an XOR gate with the resolution of 18432 bits and the PISO and SIPO registers as presented in Figure 6. The preceding section details the development of HDL code for the validation of the proposed method in real time.

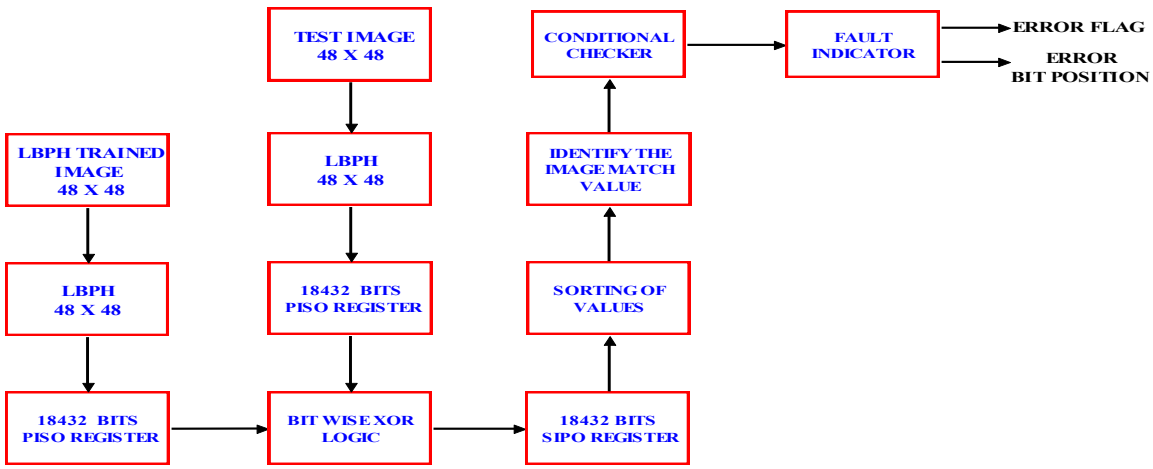

Figure 6 Block diagram for the Improved KNN algorithm to identify error pixel in LBPH image

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c. HDL Implementation of the Proposed Method

The proposed improved KNN-based error identifier for LBPH image is implemented using the Xilinx Artix 7 FPGA board. The development of HDL code for the proposed method consists of a mixed style of modelling as shown in Figure 8. The LBPH for this work is considered with the grey-scale image from the Kaggle database. Due to the limitations of the FPGA device implementation, the image resolution considered is 48 × 48 pixels. Figure 7 depicts the design flow for the proposed method. The 48 × 48 grey-scale images are converted to a hexadecimal file format using the MATLAB code. The FPGA device can only consider these 2304 pixels in a single column, with each pixel capable of accommodating a maximum of 2^8 bits of resolution. The grey-scale image with a 2^8-bit resolution considers white as 8'h00 and black as 8'hFF, respectively.

The HDL code is developed in the behavioural model to read the 2304 pixels of each 2^8 bits with a total of 18432 bits. The 18432-bit values are split into 48 rows, with each consisting of 384-bit values. The zero padding is added for the top and bottom rows, and the rightmost and leftmost columns are zero-padded. The zero padding makes the image resolution 50 × 50 pixels to manipulate the LBPH values. The LBPH calculation of the zero-padded image with 50 × 50 pixels is bit split row-wise, say Row_1-Row_3 for the 1st row of the LBPH image. Similarly, Row_2-Row_4 for the 2nd row of the LBPH image, and so on. Also, from the first 3 rows considered, $Column_1$-$Column_3$ is considered for the 1st pixel of the 1st row in the LBPH manipulation. The same pattern is followed to evaluate all the pixels of the LBPH image. To perform the LBPH calculation, the 9 pixel values from the 50 × 50 image are considered as labelled 'I_C' and 'I_0 to I_7'. The HDL code for the comparator is developed to compare the 8-bit pixel values of I_0 to I_7 with the 8-bit pixel values of I_C. Based on the condition for LBPH, the HDL code with an IF-ELSE construct is developed in a behavioural model to generate the LBPH value for each pixel.

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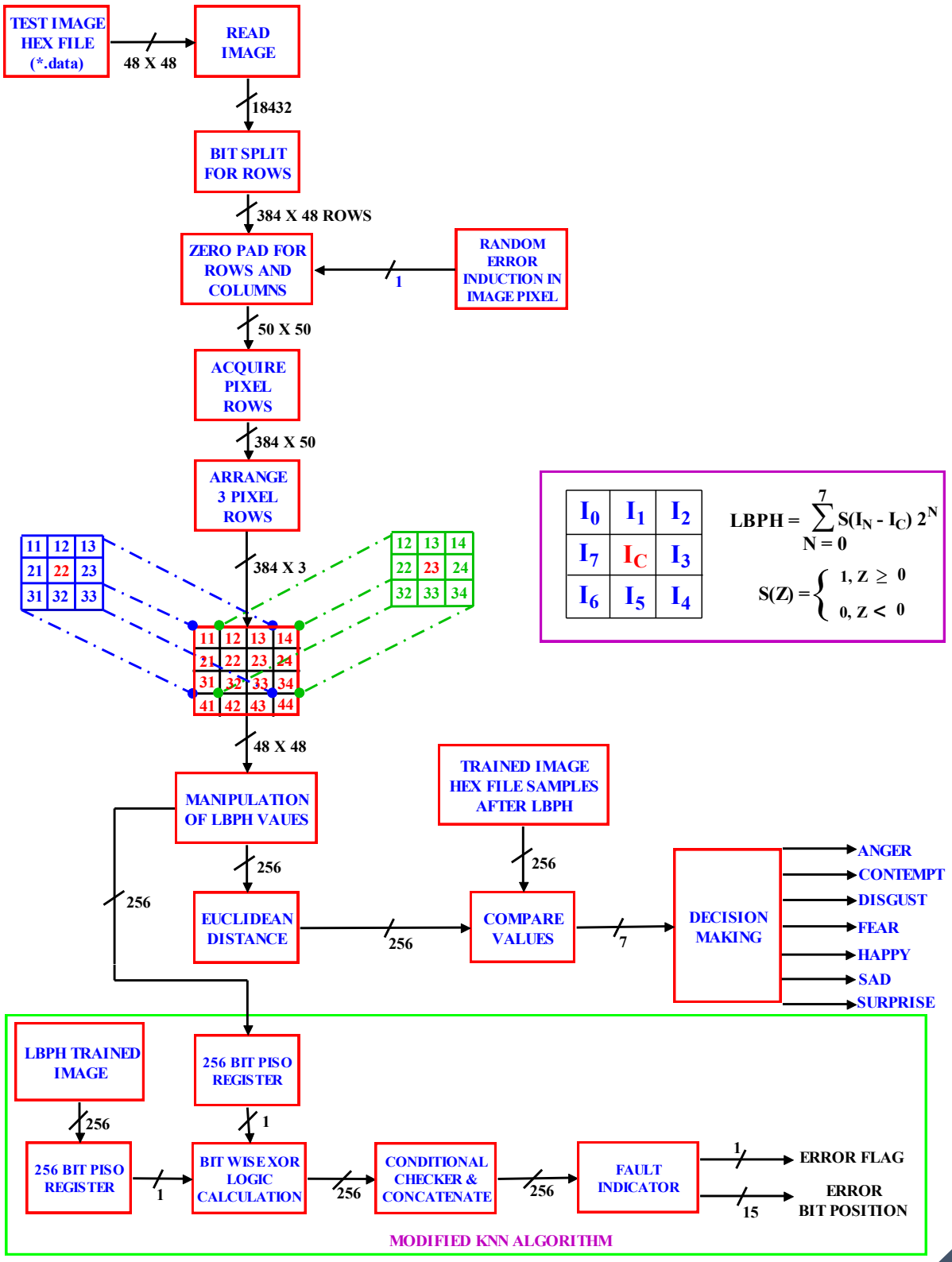

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Figure 7 HDL design flow for the proposed error analysis in LBPH using improved KNN algorithm

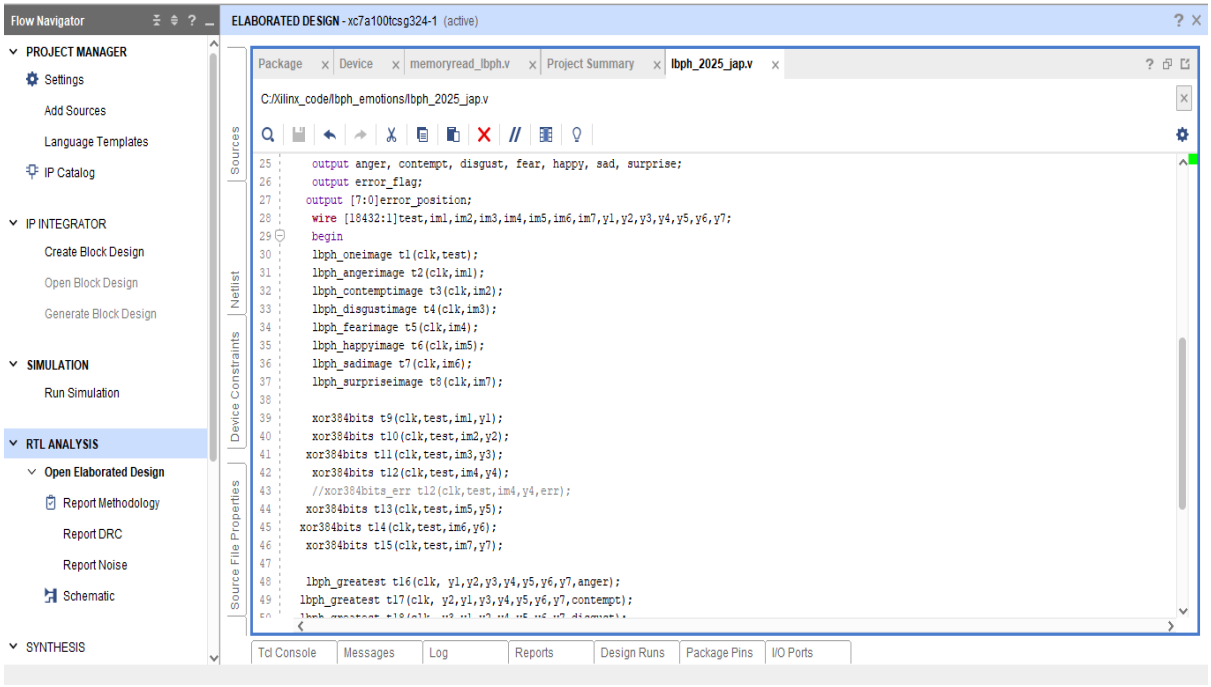

Figure 8 HDL code for the proposed fault analyser of LBPH image in Xilinx Tool

Now, the LBPH image with a resolution of 48 × 48 is generated by the developed HDL code. The histogram generation for the LBPH image includes HDL code of counters to read the number of occurrences of 8-bit values ranging from 8'h00 to 8'hFF. The proposed method aims to identify the induced error pixel in the image while comparing the test image with the trained image for the decision of emotions. To accomplish this, the error is randomly induced at the zero padding stage of the 50 × 50 resolution image. After the LBPH is generated for the test image, the LBPH for the trained sample image is compared with the test image to decide on the emotions. The Euclidean distance is calculated between the histograms of both the test image and trained samples with a resolution of 2^8-bits. The developed HDL code can compare the histogram of 1 test image and 7 trained images at a time to make an emotion decision. The compared value of the test and trained sample images that have the minimum value is considered for making an emotion decision. The random error pixel induced by 8 bits in the 50 × 50 zero-padded images is identified using the novel KNN algorithm. In the novel KNN algorithm, the test LBPH image and the trained LBPH images with 48 × 48 resolutions are sequentially considered with 1 bit to logically XOR for all the 2304 pixels. The derived XOR values will give a zero magnitude for the match of the test image to the trained image. The HDL code for the condition of least magnitude is developed, and if any single bit change has occurred, the error flag bit is activated as "1" and the corresponding bit occurrence is displayed with 2^{15} bits for the error position

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3. Results

The synthesizable HDL code for the proposed improved KNN algorithm to identify the error pixel of the LBPH image is developed and verified for its correctness. The HDL code developed for the proposed method is simulated using the Xilinx Vivado tool. Figure 9 shows the simulation output for the proposed method. The seven emotions for the proposed method are declared as binary outputs that indicate a value of '1' when active (a decision of YES) and '0' when inactive (a decision of NO). The red line partition represents the signal transition phase of the LBPH processing, followed by the error pixel identification by the improved KNN algorithm.

During the signal transition phase of the simulation, the developed HDL code retrieves the 2304 pixels from the test image as serial values. The HDL code for the LBPH image passes through zero pads and initiates the row manipulation of pixels for the 48 × 48 image. The error flag signal is used to indicate the presence of an error in the image, with the value of '1' or '0'. In the signal transition phase of the HDL code, the error flag indicates a value of '1' due to the variations in the emotion decision. These variations in the emotion outputs are the closest match between the test image and the trained image by the proposed algorithm during the transition phase. The row manipulation of the LBPH image is considered the signal transition delay. After the signal transition phase, the LBPH pixel values are generated and compared for the close match of the test and trained images. In this case, the test data image is used to decide fear. Simultaneously, the error flag is set to '0', indicating the proposed method has made an emotional decision. The time duration to make this decision depends on the resolution of the image considered and the signal transition time.

Now, for the sake of validation of the proposed method, the error pixel is induced randomly in the test image. This error pixel is induced in the zero pad stage of the LBPH algorithm and indicated as active high in the ERR signal. This induction of an error pixel in the test image will terminate the FEAR decision and represent the closed match to make the decision as ANGER. The developed HDL code of the proposed improved KNN algorithm identifies the erroneous pixel of the test image to indicate the bit pixel position as 8'h4D. The RTL schematic for the proposed algorithm proves that the developed HDL code is successfully synthesized. Figure 10 shows the RTL schematic for the proposed method using the Xilinx Tool. The area occupancy for the proposed methods utilizes only 4.78% of LUT (3031 out of 63400 available) and Flip Flops at 0.01% (7 out of 126800) when implemented in the Artix 7 FPGA device. The device utilization for the proposed method is given in Table 1. The power consumption of the proposed method using the Xilinx tool is 0.017W, as depicted in Figure 11. This is due to the low device utilization of the developed HDL code for the proposed algorithm.

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The simulation output from the Xilinx tool represents the operation of the proposed method in bit formats. To validate the genuineness of the developed HDL code of the proposed method, the generated hexadecimal file from the HDL code is cross-compiled in the MATLAB tool. The Matlab code converts the hexadecimal file to an image with the corresponding histogram of the LBPH image as presented in Figure 12. Also, the Matlab code is developed to identify

the emotion by matching the generated test LBPH image and trained LBPH image in hexadecimal to indicate the closest match of FEAR in this case. The developed HDL for the proposed method generates hexadecimal files for 1 test image and 7 trained images from each emotion. Figure 13 depicts the LBPH image of matching the test and trained LBPH image using the cross-compiling simulation in the MATLAB tool. The images used for this work are considered from the Kaggle database, with a total of 28619 trained images and 7178 test images. The test image is 25% of that of the trained image with multi-face images and 7 emotions.

Further, the developed HDL code for the proposed method is used to generate the IC layout using the Cadence EDA tool. The process of IC layout includes simulation verification using the Incisive tool, synthesizable validation using the Genus tool, and the utilization of the Net list from the Genus tool to design the IC layout. Figure 14 depicts the IC layout for the proposed method using the Cadence Innovus tool, designed using 90nm technology. Also, the proposed method is evaluated for the power consumption using the Cadence tool to exhibit a low leakage power of 1.45%. Table 2 presents the power consumption of the proposed method in the Cadence tool.

The proposed method is implemented using the FPGA device for real-time feasibility and validation. Table 3 depicts the comparison of the proposed method with the existing method in terms of VLSI parameters such as Latency, Throughput, and Power consumption. Though the resolution of the image utilized and the FPGA device selection play a vital role in FPGA-based image implementation, this comparison proves the merit of the proposed method over the other existing image-based algorithms. The FPGA Slices used for the proposed method are as low as 3059, and thus, the power consumed is 0.019W. The latency of the proposed method is 4.093 ns, compared to 9.4μs, which exhibits less timing delay due to the optimized development of the HDL code for the proposed method. The calculation of the throughput is attained by the image resolution of 2304 pixels (48 × 48) and clocking frequency of 100MHz to give a high value of 56.291Gbps.

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Figure 9 Simulation output for the proposed method using Xilinx Vivado Tool

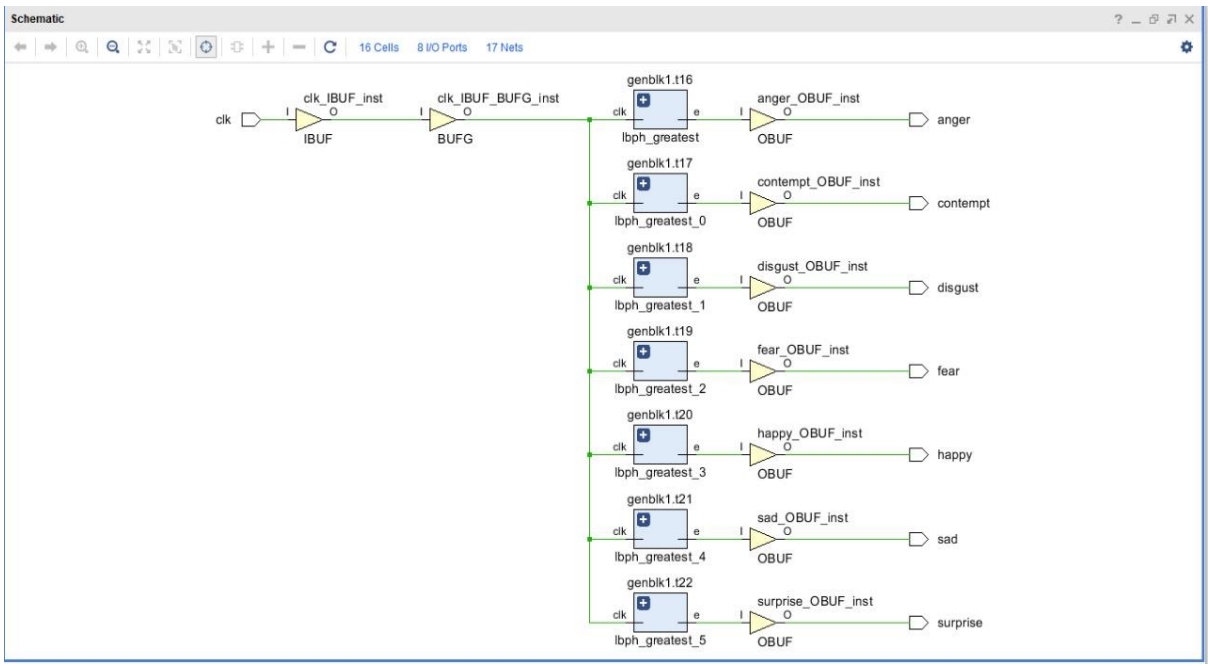

Figure 10 RTL schematic for the proposed method using Xilinx Vivado Tool

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Table 1 Device Utilization for the proposed method using Xilinx Vivado Tool

Resource	Estimation	Available	Utilization %
LUT	3031	63400	4.78
FF	7	126800	0.01
IO	8	210	3.81
BUFG	1	32	3.13

Figure 11 Power consumption for the proposed method using the Xilinx Vivado Tool

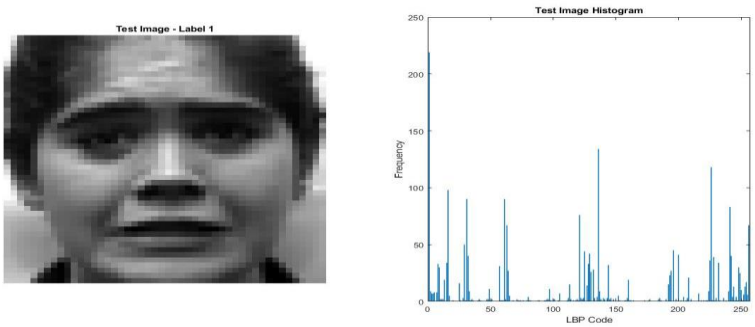

Figure 12 Cross-compiled Simulation of test image with histogram from the hex matrix generated from the developed HDL code

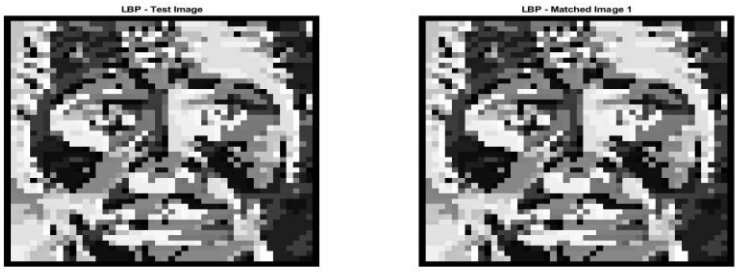

Figure 13 Cross-compiled Simulation for matching of the LBPH Test and LBPH Trained image using the hex matrix generated by the developed HDL code

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Table 2 Power consumption for the proposed method using Cadence Tool

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:        0.01885663            97.9097%
Total Switching Power:       0.00012176             0.6322%
Total Leakage Power:         0.00028082             1.4581%
Total Power:                 0.01925921
--------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Sequential                      0.01886   0.0001218   0.0002808     0.01926         100
Macro                                 0           0           0           0           0
IO                                    0           0           0           0           0
Combinational                         0           0           0           0           0
Clock (Combinational)                 0           0           0           0           0
Clock (Sequential)                    0           0           0           0           0
--------------------------------------------------------------------------------
Total                           0.01886   0.0001218   0.0002808     0.01926         100
--------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
VDD                       0.9    0.01886   0.0001218   0.0002808     0.01926         100
```

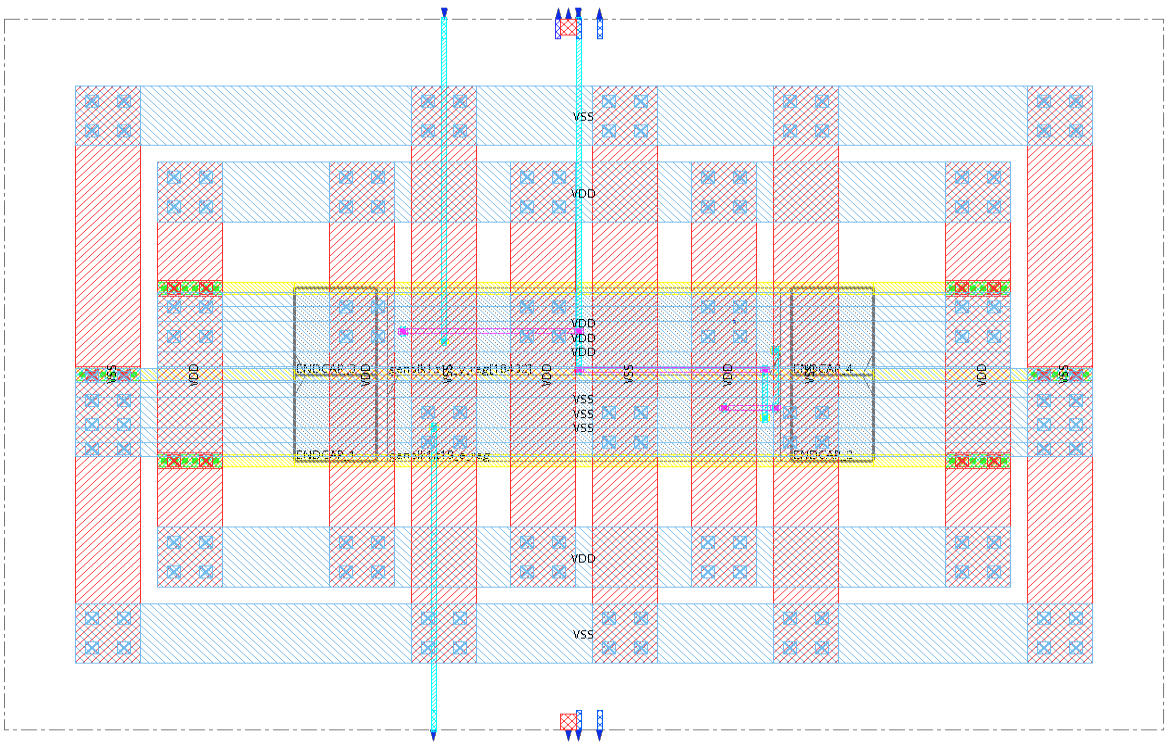

Figure 14 IC layout for the proposed method using Cadence Innovus Tool

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Table 3 Performance comparison summary of the proposed method

Ref	FPGA Device	Slices used	Latency (Clock cycles)	Through-put (Gbps)	Power (W)	Year
[20]	XC7VX690T	55769	--	--	12.21	2024
[21]	Spartan 6XC6SL45FPGA	6873	--	--	--	2024
[22]	FPGA library	121127	--	--	--	2025
[23]	Xilinx XCVU9P	3982	--	--	25	2025
[24]	Xilinx Zynq ZU7EV	196252	9.4 μs	--	1.8	2025
Ours	Artix 7 XC7A100TCSG-4	3059	4.093 ns	56.291	0.019	2025

4. Conclusion

The emotions of a multi-face human are recognized by making use of the LBPH algorithm. The test image proves the precision of recognizing all seven human emotions. The induction of error pixels in the test sample is successfully identified by making use of the improved KNN algorithm. The FPGA implementation of the proposed method exhibits superiority in terms of high throughput of 56.291Gbps with less power of 0.019W and low area. The real-time FPGA implementation of the proposed error pixel identifier proves to be feasible and easy to use. Further, the proposed methodology can be extended to high-resolution images with deep neural network algorithms for fault investigations.

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