



Control Unit of a Three-Ports Hybrid Converter of a Microgrid Based on Ternary Logic Circuits

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Abstract— This paper, provides the design and simulation of the control modes of three different power sources that are commonly used in hybrid systems especially when combining the sources of photovoltaic (PV), electric vehicles (EV) and Energy storage system (ESS). The control scenarios discuss the different combinations of sources and loads based on ternary logic system (0,1,2) that has many advantages over the classical binary logic system (0,1). To prove that, first, the ternary logic gates must be verified and simulated as MOSFET by Matlab / Simulink then a ternary logic control (TLCU) will be designed. TLCU can select the right direction of power flow from the energy source to the load based on the ternary truth table that shows the relationship between the inputs (ternary states of sources and loads) and each output that has only two states (ON or Off). At the end of the paper, the circuit of a ternary logic control circuit that can optimize the number of used elements of MOSFET is designed and tested. Comparing to binary, it is expected not only to optimize the number of MOSFET but also to accelerate the speed of operation.

Keywords—Ternary Logic TL, Hybrid System, Photovoltaic PV, Electric Vehicles EV, Energy Storage System ESS

I. INTRODUCTION

Electrical energy can be obtained from many sources such as Electric grid, photovoltaic (PV), electric vehicles (Evs), and Energy Storage (ESS). Getting energy from multiple sources in the same time is called hybrid system as shown in Fig. 1.

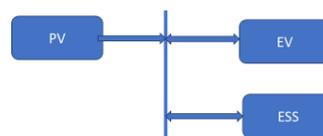


Fig 1: Hybrid System PV – EV – ESS with PI controller

In hybrid system, the main issue is how to make control between sources and loads also to determine the power flow direction from sources to exact loads especially that some sources



are considered also as load such as EV and ESS. So, it is important to determine whether the component is consuming or supplying energy. This control helps to maintain system continuity without any interruption or energy loss from the electrical network. In “Fig. 2” a hybrid system with two bidirectional and one boost inactive converter was designed [1] with proportional and integral (PI) controller.

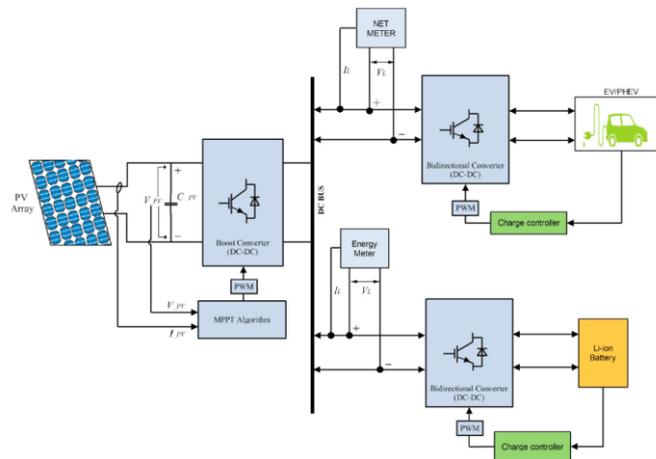


Fig 2: Hybrid System PV – EV – ESS with PI controller

In triple and double active bridge converter (TAB and DAB) with high frequency transformer [2], the control system is complicated and based on phase shift method as shown in Fig.3

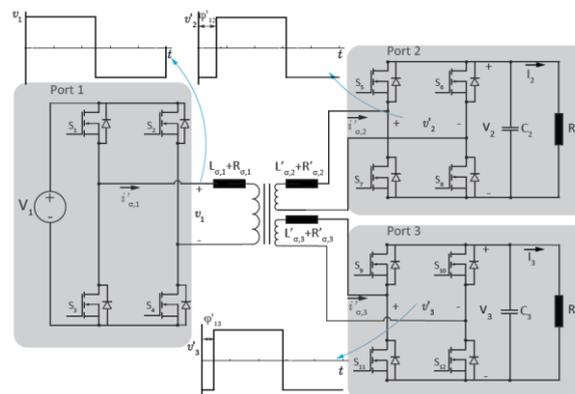


Fig 3: Hybrid System PV – EV – ESS with PI controller

II. LOGIC CONTROL OF HYBRID SYSTEM

To control multiple sources efficiently, it is necessary to use a central control unit to optimize the energy flow between sources and loads as shown in the Fig. 4.

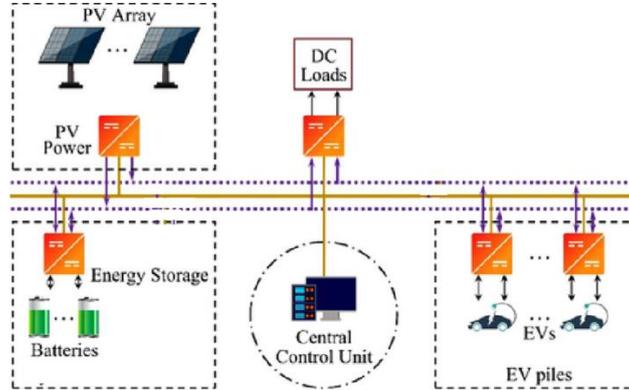


Fig. 4: Central Control of hybrid system PV – EV – ESS – Load

Due to the wide spread of multi sources energy systems, it was necessary to search for an inexpensive and uncomplicated controller that has high efficiency and suitable for small hybrid networks based on modern technology in digital systems. One of the most promising multi-valued logic systems is the Ternary logic circuits that solves most of binary problems of connection complexity and low speed of operation due to the high number of used MOSFET.

For a Triple sources hybrid system PV-EV-ESS, the desired inputs of the logic controller are described in Table 1.

TABLE I. INPUT DESCRIPTION OF SOURCES AND LOADS

Battery	state 0	Off / Battery full at rest
	state 1	Battery is Charging / or Load
	state 2	Battery is Discharge / or supply
EV	state 0	Off / EV not connected
	state 1	EV is Charging or Load
	state 2	EV is Discharge or supply
PV	state 0	PV is unavailable
	state 1	PV is Available for Batt or EV Only / priority for battery
	state 2	PV is Available for Battery & EV

A Ternary Logic Control Unit TLCU is the proposed solution for controlling hybrid system of multi-energy sources. The design of such logic controller must study the inputs of hybrid system (PV, EV, and ESS) analyzes it, and gives the optimum output of the combined energy sources to obtain an optimum power flow as shown in Fig. 5.

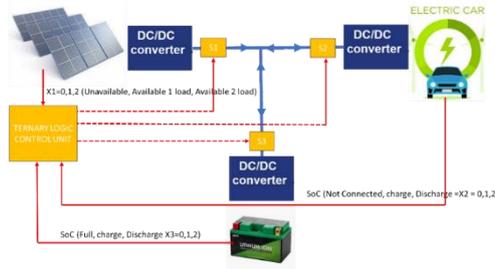


Fig. 5. Block diagram of PV, EV, ESS system

Table II, provides a list of the modes of operation as ternary truth table that relates the inputs to the outputs of sources

TABLE II. INPUT DESCRIPTION OF SOURCES AND LOADS

MODES OF OPERATION						
X1	X2	X3	Mode	PV	EV	BT
Source	Source/ Load	Source / Load		S1	S2	S3
PV	EV	BT				
0	0	0	OFF	0	0	0
0	0	1	Infeasible = Alarm Mode	0	0	0
0	0	2	Infeasible	0	0	0
0	1	0	Infeasible	0	0	0
0	1	1	Infeasible	0	0	0
0	1	2	EV charging from Battery	0	1	1
0	2	0	Infeasible	0	0	0
0	2	1	Battery charging from EV	0	1	1
0	2	2	Infeasible	0	0	0
1	0	0	Infeasible	1	0	0
1	0	1	Battery Charging from PV	1	0	1
1	0	2	Infeasible	1	0	0
1	1	0	EV charging from PV	1	0	0
1	1	1	EV & Battery charging from PV / EV to be off	1	0	1
1	1	2	EV charging from PV & Battery	1	1	1
1	2	0	Infeasible	1	0	0
1	2	1	Battery Charging from PV and EV / EV to be off	1	0	1
1	2	2	Infeasible	1	0	0
2	0	0	Infeasible	1	0	0
2	0	1	Battery Charge from PV	10	0	10
2	0	2	infeasible	1	0	0
2	1	0	EV charging from PV	1	1	0
2	1	1	EV & Battery charging from PV	1	1	1
2	1	2	EV charging from PV / Bat to be off	1	1	0
2	2	0	Infeasible	1	1	0
2	2	1	Battery charging from PV / EV to be off	1	0	1
2	2	2	Infeasible	1	0	0



III. BINARY AND TERNARY LOGIC SYSTEMS

The well-known finite set of binary system is:

$$E(2) = \{0, 1\} \quad (1)$$

Also, the ternary system deals with finite set of values as follows:

$$E(3) = \{0, 1, 2\} \quad (2)$$

The same type of positional notation is used in the ternary number system as in the decimal system. Table III, lists the first 10 ternary numbers and their equivalents in binary and decimal.

TABLE III. DECIMAL, BINARY AND TERNARY NUMBERS

Decimal	Binary	Ternary
0	0000	00
1	0001	01
2	0010	02
3	0011	01
4	0100	10
5	0101	11
6	0110	12
7	0111	20
8	1000	21
9	1001	22

In control system, the advantage of ternary over binary is that can provide more addresses with fewer address lines. Example to send the decimal data 9, it needs 4 addresses in binary while 2 lines are enough in ternary. The ternary arithmetic and algebra can be treated in the same way of the binary. The ternary logic algebra could be introduced through the following two formulations [4]. The usual rules for the operations:

- TAND (The minimum between variables, denoted by \wedge or \bullet)
- TOR (The maximum between variables, denoted by \vee or $+$)
- The evaluation rules for the disjoint operations C_0 , C_1 , and C_2 for a given ternary variable $x = \{e_0, e_1, e_2\}$ is given in Table II:



TABLE IV. EVALUATION RULE FOR DISJOINT OPERATION FOR N=3

X	$C_0(X)$	$C_1(X)$	$C_2(X)$
e_0	e_2	e_0	e_0
e_1	e_0	e_2	e_0
e_2	e_0	e_0	e_2

Using the disjoint operations C_0, C_1 and C_2 , the disjunctive normal form for any ternary switching function is obtained as easily as in the binary case. For one variables X , the switching function is:

$$f(X) = [f(e_0) \wedge C_0(X)] \vee [f(e_1) \wedge C_1(X)] \vee [f(e_2) \wedge C_2(X)] \quad (3)$$

IV. TERNARY LOGIC GATES

A. Ternary Inverter

The inverter in ternary can be defined as the ternary complement of the input signal.

$$Y = \bar{X} = 2 - X \quad (4)$$

The symbol and truth table of Ternary NOT gate are shown in Fig. 6 and Table V.



Fig. 6: Ternary NOT gate

TABLE V. TRUTH TABLE OF TERNARY INVERTER

X	NOT
0	2
1	1
2	0

Using Simulink Matlab, STI (Simple Ternary Inverter): Constructing of each block from the complete circuit in Fig. 7 [3] where the applied logic voltages in simulink are {0V, 5V, 10V} which complies with ternary set {0,1,2}

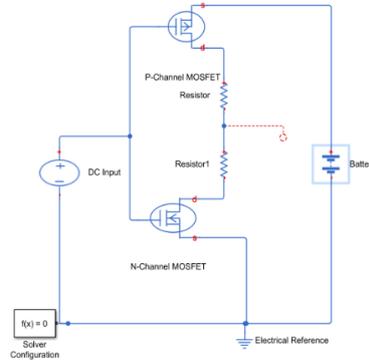


Fig. 7: Electronic Circuit of STI in Simulink

The Negative Ternary inverter (NTI) IS shown in Fig. 8. by using Matlab/ Simulink [3]

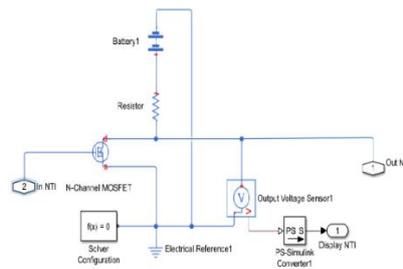


Fig. 8. Schematic diagram shows the PTI in Simulink

The Positive Ternary inverter (PTI) is shown in Fig. 9 by using Matlab/ Simulink [3].

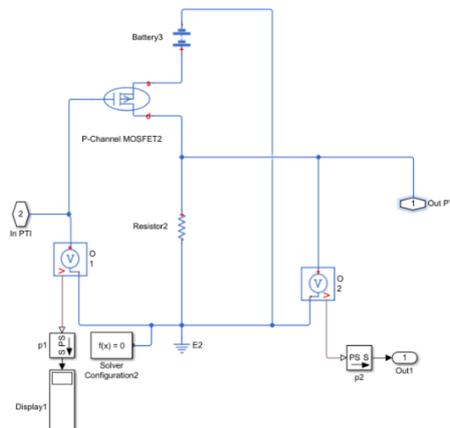


Fig.9 Schematic diagram shows the PTI in Simulink



B. OR and AND Gates in Ternary System

For TOR, The output signal is equal to the greatest input while for TAND, the output is the minimum between the inputs

TOR equation

$$Y = A + B \quad (5)$$

TAND equation

$$Y = A.B \quad (6)$$

The TNOR and TNAND are the inverted values of TOR and TAND The following truth tables

TABLE VI. TRUTH TABLE OF TOR, TNOR, TAND, TNAND

A	B	TOR	TNOR	TAND	TNAND
0	0	0	2	0	2
0	1	1	1	0	2
0	2	2	0	0	2
1	0	1	1	0	2
1	1	1	1	1	1
1	2	2	0	1	1
2	0	2	0	0	2
2	1	2	0	1	1
2	2	2	0	2	0

The logic symbols of logic gates

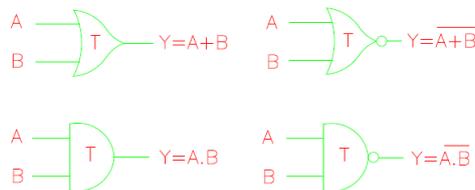


Fig. 10: The Ternary TOR, TNOR, TAND and TAND3

The Matlab / Simulink circuits of TNOR and TNAND are shown respectively in figures 11 and 12.

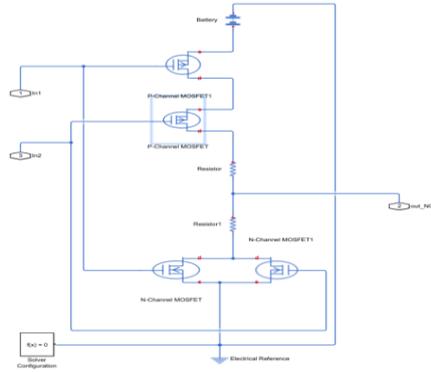


Figure 11. Matlab / Simulink circuit of TNOR gate

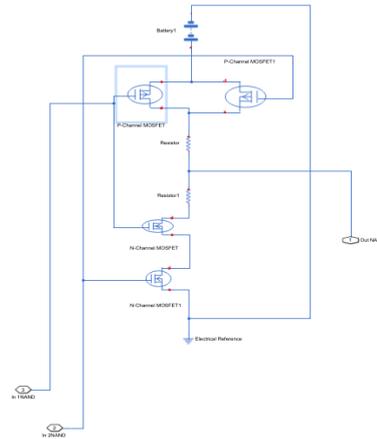


Fig. 12: Matlab / Simulink circuit of TNAND gate

C. Design of Ternary Address Control Unit TACU

The main goal of designing the Ternary Address Control Unit (TACU) is through one control variable 'A' there will be three states, and in each state, it must represent one input and omit the others. This will lead to think again about ternary algebra and its properties especially the equation of switching function [5].

$$F(A) = [X0.C_0(A)] + [X1.C_1(A)] + [X2.C_2(A)] \quad (7)$$

Where $C_0(A)$ $C_1(A)$ $C_2(A)$ are three control lines taking each three values according to A as on the Table VII:

TABLE VII. EVALUATING RULE FOR DISJOINT OPERATION

A	$C_0(A)$	$C_1(A)$	$C_2(A)$
0	2	0	0
1	0	2	0
2	0	0	2



The block diagram of TACU with logic circuit to select one of three inputs X1, X2 and X3 is shown in Fig. 13 and the Matlab circuit is shown in Fig. 14.

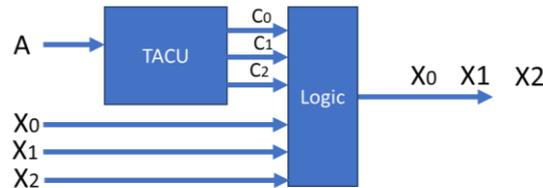


Fig. 13: Block Diagram of TACU and three inputs

if $A = 0$ then $f(A) = X_0.C_0(0) + X_1.C_1(0) + X_2.C_2(0) = X_0$
 if $A = 1$ then $f(A) = X_0.C_0(0) + X_1.C_1(0) + X_2.C_2(0) = X_1$
 if $A = 2$ then $f(A) = X_0.C_0(0) + X_1.C_1(0) + X_2.C_2(0) = X_2$

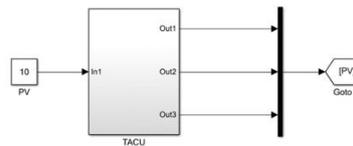


Fig. 14: Matlab circuit of Block of TACU

The complete Matlab / Simulink circuit that satisfies the table V using MOSFET transistor MATLAB SIMULINK

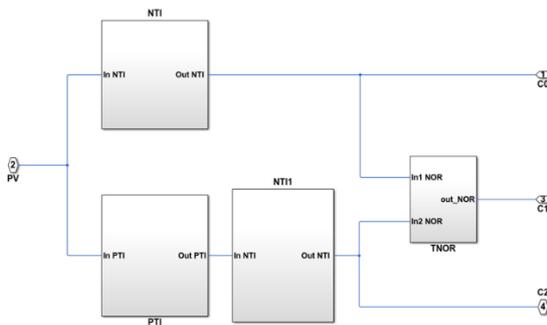


Fig. 15 Matlab circuit of TACU using MOSFET

The circuit includes 2x NTI and 1xPTI and 1xTNOR

V. DESIGN OF A TERNARY LOGIC CONTROL UNIT FOR HYBRID POWER SYSTEM WITH THREE SOURCES

To design the TLCU that makes the full control between sources and loads and that can make the energy management, it is necessary to refer back to Table II where it is needed to find



the equations of the outputs S1, S2 and S3 as ternary functions of the inputs X1, X2 and X3. For this purpose, the truth tables are presented with the simplified equations.

TABLE VIII. TRUTH TABLE OF S1

	x2.x3											
x1	0 0	0 1	0 2	1 0	1 1	1 2	2 0	2 1	2 2	2 2	2 2	2 2
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	1

Based on the table VIII, the simplified equation of S1 using the ternary Karnaugh map is,

$$S1 = C_1(X_1) \text{ TOR } C_2(X_1) = C_{12}(X_1) \quad (8)$$

TABLE IX. TRUTH TABLE OF S2

	x2.x3											
x1	0 0	0 1	0 2	1 0	1 1	1 2	2 0	2 1	2 2	2 2	2 2	2 2
0	0	0	0	0	0	1	0	1	0	0	0	0
1	0	0	0	0	0	1	0	0	0	0	0	0
2	0	0	0	1	1	1	1	1	0	0	0	0

Based on the Table IX, the simplified equation of S2 using Ternary Karnaugh map is,

$$S2 = C_2(X_1) \text{ TAND } [C_1(X_2) \text{ TAND } C_{01}(X_3) \text{ TOR } C_2(X_2) \text{ TAND } C_0(X_3)] \text{ TOR } C_0(X_1) \text{ TAND } C_2(X_2) \text{ TAND } C_1(X_3) \text{ TOR } C_1(X_2) \text{ TAND } C_2(X_3) \quad (9)$$

TABLE X. TRUTH TABLE OF S3

	x2.x3											
x1	0 0	0 1	0 2	1 0	1 1	1 2	2 0	2 1	2 2	2 2	2 2	2 2
0	0	0	0	0	0	1	0	1	0	0	0	0
1	0	1	0	0	1	1	0	1	0	0	0	0
2	0	1	0	0	1	0	0	1	0	0	0	0

Based on the Table X, the simplified equation of S3 using Ternary Karnaugh map is,

$$S3 = C_{12}(X_1) \text{ TAND } C_1(X_3) \text{ TAND } C_{01}(X_2) \text{ TOR } C_{01}(X_1) \text{ TAND } C_1(X_2) \text{ TAND } C_2(X_3) \text{ TOR } C_2(X_2) \text{ TAND } C_{01}(X_3) \quad (10)$$



Combining S1, S2 and S3, then the general diagram of the TLCU becomes as given and proved in Matlab / Simulink in Fig. 10.

VI. TERNARY RESULTS WITH COMPARISON WITH BINARY

The total number of MOSFET is very important since it determine the dimensions of any logic integrated circuits [5]. Based on the simulation of ternary logic gates and the equations (9,10,11) and the block diagram in Fig. 10 , it is found that the total number of NMOS and PMOS of the logic unit TLCU can be calculated as follows:

- 1) 6 x NTI each has one NMOS
- 2) 3 x PTI each has one PMOS
- 3) 6 x TNOR each has 2 NOMS and 2 PMOS
- 4) 6 x TOR each has 3 NMOS and 3 PMOS
- 5) 14 xTAND each has 3 NMOS and 3 PMOS

Then the total number of MOSFET is 78 x NMOS and 75 PMOS. To see whether the design is effective or not, a comparison with binary system is necessary. The simplified equation of S1, S2 and S3 based on 6 input variables shows that total number of MOSFET are 146 x NMOS and 146 PMOS (refer to appendix to check the total number of MOSFET in binary through the equations of S1, S2 and S3)

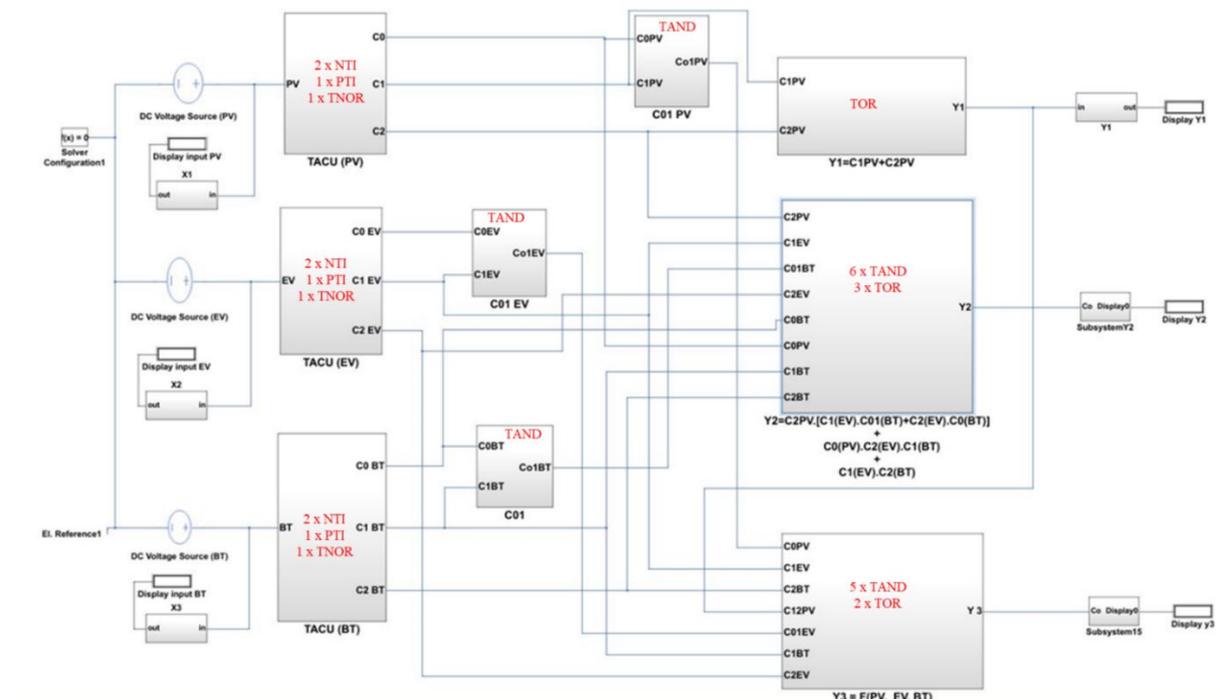


Fig. 16. Matlab circuit of Block of TACU



APPENDIX

Binary Karnaugh map and equation of S1 (Bold letter = NOT)

X1	X2,X3			X2,X3														
B1 B0	B1 B0 B1 B0																	
0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

$S1 = \overline{B0(X1)} \cdot B1(X1) + B0(X1) \cdot \overline{B1(X1)}$ > (.) indicate AND ; (+) indicate OR

Binary Karnaugh map and equation of S2 (Bold letter = NOT)

X1	X2,X3			X2,X3														
B1 B0	B1 B0 B1 B0																	
0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

$S2 = B0(X1) \cdot B1(X1) \cdot [B0(X2) \cdot B1(X2) \cdot B1(X3) + B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3)] + B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3) + B0(X1) \cdot B1(X1) \cdot B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3)$

Binary Karnaugh map and equation of S3 (Bold letter = NOT)

X1	X2,X3			X2,X3														
B1 B0	B1 B0 B1 B0																	
0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

$S3 = [B0(X1) \cdot B1(X1) + B0(X1) \cdot B1(X1)] \cdot [B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3) + B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3)] + [B0(X1) \cdot B1(X1) \cdot B0(X1) \cdot B1(X1)] \cdot [B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3) + B0(X2) \cdot B1(X2) \cdot B0(X3) \cdot B1(X3)]$

VII. CONCLUSION

A ternary logic control unit is presented with effective number of MOSFET comparing to binary approximately saving the half of MOSFET need number. This will lead to minimize the heat losses inside the controller and will optimize the cost and will minimize the size and dimensions of controller also will minimize the complexity of connections as it will be so hard for the large number of transistors in binary comparing to half number in ternary. The ternary logic seems very good solution for such problems in binary as it provides large amount of data with less number of address lines. The ternary logic fits very well the control of three ports hybrid converter and applies all its advantages when designing the TLCU. Finally, the simulation of MATLAB / Simulink helps also to provide additional optimization and helps to verify the results of simplified ternary equations of switches of the hybrid system. This method can be applied for superior number of hybrid sources such as PV – EV – ESS – Grid – Gen – Load in this case a multivalued logic with higher base (quaternary, quinary or even octal) can be used to simplify the number of combinations and connections.

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