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A Bootstrapped Domino Logic–Based Schmitt Trigger for Low-Power and Noise-Immune Power System Applications

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Abstract*:* The Schmitt trigger is one of the most important components of electronic systems that are used to monitor and control the power supply's voltage. Using the Schmitt trigger allows to filter out unwanted noise, thus improving the quality of signal. Traditional CMOS-based Schmitt triggers were limited in speed and exhibited excessive leakage power and a degraded performance when operating at lower voltages, thus making them unsuitable for advanced digital circuit applications such as the monitoring and control of the electrical distribution systems. This work presents Bootstrapped Dynamic Logic Schmitt Trigger (BSD-ST) using the FinFET technology of 18nm for high-speed operation, low leakage power, and improved noise immunity when operating in subthreshold voltage conditions. The proposed circuit functions in dual modes - in Schmitt trigger mode and a domino logic gate through a select input. Simulation results using Cadence Virtuoso show a 47MHz switching speed, 0.94nW leakage power, and 25mV hysteresis width. This design is ideal for applications where low power, high speed and tolerance to noise are paramount, including power systems and protection circuits, and devices with low voltages and high noise environments.

Keywords: Schmitt trigger, leakage power, Bootstrapped, noise immunity, hysteresis

1. INTRODUCTION

The use of high-speed digital and mixed-signal electronics has increased in modern power systems for monitoring, protecting and controlling these systems. Power electronic converters have a high level of switching activity which generates noise and electromagnetic interference that can interfere with the sensor outputs, resulting in incorrect sensor outputs, and improper operation of the system [1].

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Schmitt triggers are used in these types of mixed-signal environments with a high noise level to switch signals based on thresholds with hysteresis. They are also employed in zero-crossing detectors and comparators in protection applications, pulse-shaping and reliable control signal generation in pulse-width modulation controllers and input conditioning of signals into analogue-digital converters [2-4]. Consequently, Schmitt triggers are highly suitable for use in modern scaled CMOS/FinFET technologies, which are subject to increased amounts of noise and variability.

However, the traditional CMOS Schmitt Trigger design has significant challenges with advanced technology nodes, particularly in the sub-threshold region. In the sub-threshold region, the drive strength is reduced, leakage currents are increased, and switch speeds are limited, negatively affecting the performance of Schmitt Triggers using bulk CMOS [5]. These limitations are critical for applications in high-noise or rapid-transient environments. FinFET-based Schmitt Trigger designs provide reliable performance within the sub-threshold region [6].This work proposes a BDL-ST, operated in subthreshold region utilizing 18nm FinFET technology [7-8]. The circuit combines capacitive bootstrapping with dynamic domino logic. The BDL-ST circuit is capable of dual-mode operation via a control signal, allowing it to behave as a conventional Schmitt Trigger for noise-tolerant conditioning of signals, or as a dynamic domino gate for high-speed evaluation.

2. SUBTHRESHOLD FinFET TECHNOLOGY FOR SCHMITT TRIGGER APPLICATIONS

i. FinFET Technology

CMOS technology is approaching its scaling limits (i.e. below 32 nm), traditional planar MOSFETs are affected by tremendous short-channel effects (SCEs), increased leakage currents, reduced gate control and so on. In order to mitigate these issues, a new technology referred to as Fin Field Effect Transistor (FinFET) has been developed to offer a new way of implementing multigate transistor based architecture. When compared to planar MOSFETs, FinFETs exhibit significant improvement in the ratio of current on to off (Ion/Ioff), lower gate capacitance , steeper subthreshold slopes, improve immunity to random dopant fluctuation, enable the continued scaling of devices, and enable lower power consumption, all of which serve to extend Moore's Law for future generations of nanoscale semiconductor devices[9].

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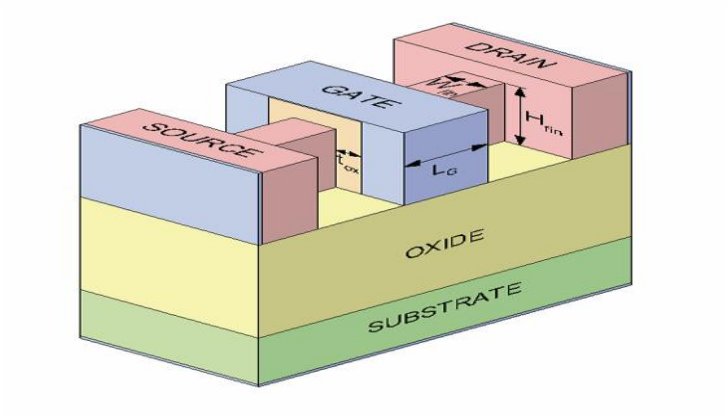

Fig.1. Schematic representation of the basic FinFET structure

The FinFET structure as depicted in Fig.1 can be represented as a regular MOS transistor that has been rotated by 90 degrees about its drain to source axis, giving rise to a non-planar transistor structure in a wrapped-gate configuration. Whereas planar MOSFETs have horizontally oriented channels, FinFETs have vertically oriented channel "fins"[10]. The gate structure in FinFETs wraps around the channel on multiple sides creating better electrostatic control of charge transport. When considering FinFET structures, the critical fin dimensions are basically fin height (H_{fin}) and fin width (W_{fin}). The fin height resembles to channel width of a planar MOSFET, which has a major influence on drive current and performance. The channel length in a FinFET is determined by the length of the gate, while the effective width of the channel is defined by the total perimeter of the channel that is located beneath the influence of gate control and this is expressed as:

$$W_{eff} = 2H_{fin} + T_{fin} \quad \text{-------- (1)}$$

T_{fin} represents the thickness of the fin and if the number of fins is increased then more effective channel width is created, leading to added channel charge density and better electrostatic gate control, thus improving device performance. However, mechanical instability and decreased reliability will result from fabrication constraints and variability due to processing, which limit the height of fins to an optimum level.

ii. FinFET Technology in the Subthreshold Region

Subthreshold operation is achieved in the regime where the supply voltage is lower than the threshold voltage of a device and the sub-threshold leakage current can be used as its operating current. While much work has been conducted on the use of sub-threshold operation in bulk CMOS technologies, their inefficiency due to inadequate electrostatic control limits their potential for use in ultra-low-power applications. The limitations of planar transistors are effectively addressed by FinFET technology in the subthreshold region [11-12].

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Within the subthreshold region of FinFET operation, total energy consumed consists of both dynamic and leakage energy components; Dynamic energy can be expressed mathematically as follows:

$$E_{dyn} = \alpha C V_{DD}^2 \quad \text{--------} \quad (2)$$

Where α indicates the activity factor, C is the total switching capacitance of the circuit, and V_{DD} is the power supply. The fundamental equation governing sub-threshold current is

$$I_{sub} = K e^{\frac{V_{gs}-V_{th}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}}) \quad \text{----}$$

---- (3)

Where V_T is the thermal voltage which is temperature dependent, K is a technology associated parameter, n is the subthreshold slope and V_{th} is the threshold voltage.

The total energy is given by

$$E_{total} = E_{dyn} + E_{leak} = \alpha C V_{DD}^2 + I_{leak} V_{DD} T_{delay} \quad \text{----}$$

---- (4)

Where I_{leak} signifies the leakage current and T_{delay} is the circuit delay.

Dynamic energy consumed by a circuit will continue to decrease as the supply voltage decreases while it is operating in the subthreshold region; however, in this region, subthreshold leakage current acts as a driving current and will cause T_{delay} to increase greatly as the voltage decreases further.

iii. Subthreshold FinFET Schmitt Trigger

By lowering supply voltage and power consumption, subthreshold (weak inversion) operation is becoming the mainstream technique used in the development of ultra-low-power electronic systems. Unfortunately, circuits that operate in this region are more susceptible to noise , process variations and fluctuations in supply voltage than circuits that conduct current through stronger inversion. They also have degraded frequency response and linearity and as such will only be useful in low-frequency and low-power applications. The application of FinFET-based Schmitt Triggers provides increased switching robustness in subthreshold operation [13] because multigate FinFET exhibit superior electrostatic control, mitigating short-channel effects. In Schmitt triggers the inherent hysteresis (i.e., positive feedback) produces two different threshold voltage levels for rising and falling transitions that eliminate switching caused by noise and increase the static noise margins. Thus, the dual-threshold characteristic of Schmitt triggers provides the capability to eliminate noise-induced switching and restore signal integrity in both Analog and Digital Circuits.

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3. PROPOSED BOOTSTRAPPED DOMINO LOGIC SCHMITT TRIGGER

The BDL-ST design presented in this article integrates the concepts of bootstrapping, domino Logic, and Schmitt trigger hysteresis. The trailblazing elements that characterize the proposed design are dynamic switch action combined with capacitive bootstrapping, which also include positive feedback. As a result, the design archives high-quality switching performance while maintaining robustness against noise arising from supply and input signal fluctuations.

The BDL-ST circuit has a control signal (S) to switch between Schmitt trigger and domino logic modes [14]. The circuit has a control module and the dynamic Schmitt trigger core allows for adaptability between a noise-resistant signal conditioning circuit and fast logic evaluation.

i. Bootstrapping Capacitor Configuration

Bootstrapping is achieved through capacitor connections to the gate of critical transistors that provide temporary increases in gate-source voltage at the time of the switching state. This dynamic enhancement of the gate-source voltage enhances drive strength; decreases propagation delay, and improves the sharpness of the turn-on and turn-off transitions under low supply voltages, for this reason, the bootstrapped capacitors are able to speed up both the pull-up and pull-down transitions and do not permanently increase power consumption.

ii. Logic Operation as Domino mode

In the domino logic mode, S=1, the circuit has two phases, which can be controlled by the clock signal. In the first phase (CLK = 0), the dynamic node of the circuit has been set to a predetermined state prior to the start of the evaluating phase. In the second phase (CLK = 1), the evaluating circuit is activated, and logic is generated by both the current input signals and the charge stored on the dynamic node. Dynamic operation reduces static power dissipation so that higher frequency operation is allowed in synchronous digital designs.

iii. Operation as a Schmitt Trigger mode

If S=0 the multiplexer allows Vin to control the circuit operates as a Schmitt Trigger. The Schmitt Trigger uses positive feedback within the core and thereby adds hysteresis to the input signal, creating a separation between a rising and falling threshold voltage level. This helps in eliminating noise and allows for a slow or noisy input transition to not cause a spurious output. The Fig.2. illustrates the bootstrapped domino logic Schmitt Trigger.

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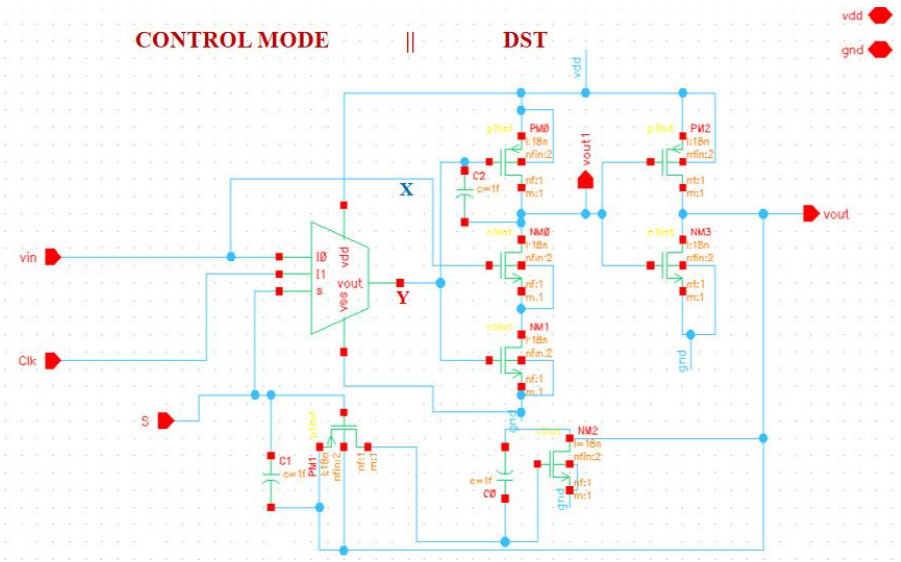

Fig.2. Schematic of Bootstrapped Domino Logic Schmitt Trigger

A circuit is made up of two main sections: the control section and the Dynamic Schmitt Trigger (DST) Section. The control section includes a multiplexer (MUX) that chooses either the input signal (Vin) or clock based on the control signal (S), thus determining if the circuit operates in the Schmitt Trigger or Domino logic modes. When "S=0", the multiplexer routes the input signal (Vin) to node (Y) and, thus, activates the Schmitt trigger mode of operation. In contrast, when "S=1", the multiplexer routes the clock signal to node (Y) and, thus, activates the domino logic mode of operation. The transistor MP1 acts to either pre-discharge the control signal pathway or isolate it depending upon the logic control. Capacitor (C1) is connected at the gate of transistor MP1 to improve the speed of the switching operation and reduce the switching delay.

The Schmitt trigger's pull-up/pull-down network consists of transistors PM0, NM0, and NM1 in the DST section. While MP0 is conductive (ON) and keeping node Vout1 at Vdd a high state, at the same time NM0 and NM1 are non-conductive (OFF). Transistor PM0's gate is energized by capacitor C2 attached between its gate and source terminal, thereby enhancing the transition speed of Vout1 as it is charged up due to bootstrapping increasing the gate drive current into PM0. Once node Y transitions to a high state, both NM0 and NM1 become conductive while PM0 becomes non-conductive, causing Vout1 to transition from high to low. At this point, NM2 is activated and, therefore, will charge the capacitor C0. The capacitor will temporarily store the charge and forward the charge onto the input of the NM2 in order to exert a reinforcing action on the falling edge of Vout1. The stored charge will discharge node Vout1 very quickly through NM2, thereby increasing the noise immunity and speed of the circuit.

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The inverter receiving its input from PM2 and NM3 produces Vout, which exhibits the processed and sharpened digital signal. The bootstrapped design improves speed and reduces delay in combination with enhancing the signal quality when utilised in low voltage environments due to the effect of capacitive acceleration produced by C0 and C2. This circuit also benefits from both dynamic and Schmitt trigger operation modes enabling dual mode operation for greater robustness in high-speed digital. The performance of the BDL-ST is compared with the Conventional Schmitt Trigger [13], the bootstrapped Schmitt Trigger[7], and the domino logic Schmitt trigger [14]

4. RESULT AND ANALYSIS

All of the circuits were designed and simulated with Cadence Virtuoso by utilizing the 18 nm FinFET transistor process design kit (PDK) at a typical process corner and at 27 ^{o}C. The supply voltage was set to 0.3 V, which is less than the nominal FinFET threshold voltage range ($V_{th,n} \approx 0.35–0.45$ V and $|V_{th,p}| \approx 0.40–0.50$ V). This guaranteed that all circuits will operate in the subthreshold region with improved energy efficiency and robustness.

Parameter Evaluation Methodology:

Dynamic Power: Average of the supply current during active switching taken from a transient analysis method was used to measure.

Leakage Power: Using either DC or transient simulation, the steady-state supply current (with static input) was used to obtain leakage power.

Switching Speed: The maximum functional frequency at which the output transitions maintained correct flipping is considered the switching speed, as determined by transient simulations.

Propagation Delay: The delay was determined as an average of the two delays, low-to-high and high-to-low, measured as the difference in time from 50% voltage rise point of the input and 50% voltage fall point of the output waveforms.

Power-Delay Product (PDP):

Calculated as follows

$$PDP = P_{avg} \times t_{pd}, \quad \text{---------- (5)}$$

where P_{avg} is the average power and t_{pd} is the propagation delay.

Hysteresis Width:

Also obtained from DC transfer characteristics by sweeping the input voltage in both the forward and reverse direction, and measuring the voltage difference between the rising and falling switching threshold.

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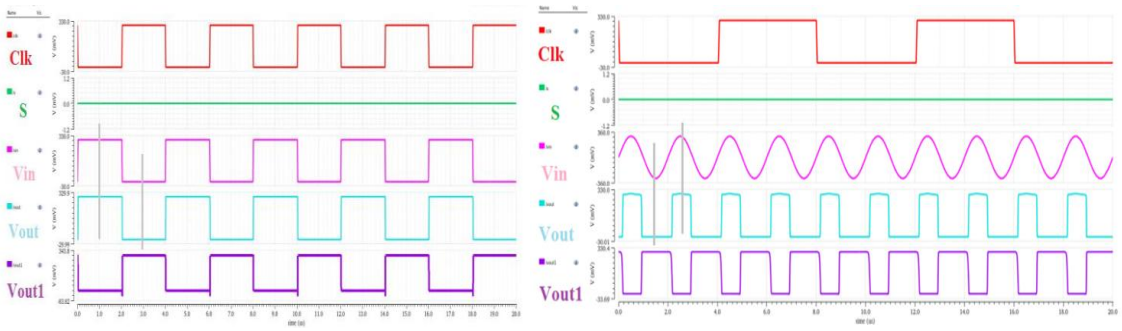
Noise Margin: Obtained from the VTC by determining the high and low noise margins (NMH and NML), since Schmitt trigger circuits have a hysteresis window the Noise Margins are enhanced.

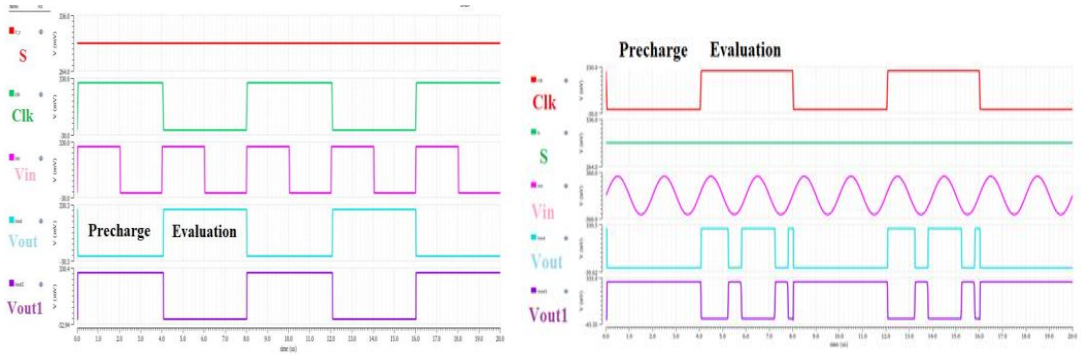
Fig. 3. shows the transient response of the bootstrapped domino logic Schmitt trigger when S = 0 for two different types of input voltage. The circuit operates as a Schmitt trigger when S is 0, as Vout will track Vin regardless of the state of the clock signal. Therefore, this demonstrates that the Schmitt trigger is functioning properly.



(a) (b)

Fig.3. Transient response of bootstrapped domino logic Schmitt trigger for S=0: (a) pulse input and (b) sinusoidal input

Fig.4 shows that for S = 1, the circuit operates in domino logic mode with two phases; precharge (CLK = 0) and evaluate (CLK = 1). The output voltage (Vout1) will remain precharged while the clock signal is low (CLK = 0), and its only change occurs when the clock signal goes high (CLK = 1).During this second phase, the output voltage will change based upon the voltage level present at the input.



(a) (b)

Fig.4. Transient response of bootstrapped domino logic Schmitt trigger for S=1: (a) pulse input and (b) sinusoidal input

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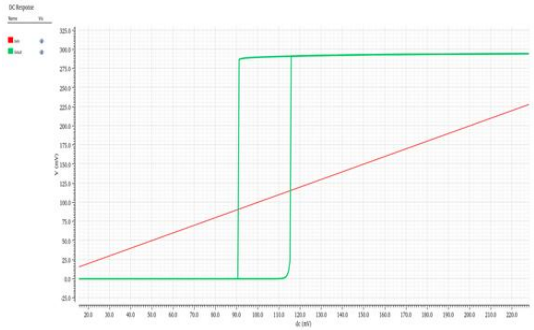

Fig.5. Fig. DC Transfer characteristics of bootstrapped domino logic Schmitt trigger.

According to Fig.5. the Schmitt trigger has two defined switching thresholds (V_{HL} and V_{LH}). V_{HL}occurs during the first rising transition and V_{LH} is triggered during the second fall-off transition of Vin. The hysteresis width is the difference between the upper (V_{HL}) and lower (V_{LH}) thresholds. The existence of a hysteresis area shows that the positive feedback has been effectively employed to maximize the Schmitt trigger ability to overcome noise, creating a stable switching point to enable improved performance overall.

Table 1 provides a summary of the performance for the Schmitt Trigger topologies examined in the subthreshold domain.

Table 1: Performance comparisons of different Schmitt trigger topologies

Parameter	Conventional Schmitt Trigger[ST]	Bootstrapped Schmitt Trigger[BST]	Domino Logic Schmitt Trigger [DL-ST]	Bootstrapped domino logic Schmitt trigger BDL-ST
Dynamic power(nW)	0.523	0.76	0.97	1.40
Leakage power(nW)	1.05	1.48	1.91	0.94
Switching peed(MHz)	58	79	13	47
PDP(pJ)	4.45	4.77	35.114	15.56
Hysteresis width(mv)	96	9.62	30	25
Noise margin(V)	0.09	0.18	0.18	0.19

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The bar chart depicted in Fig.6. is based on the data provided in Table 1 and allows visual comparison of the different metrics associated with Dynamic power, Leakage power, switching speed, PDP, Hysteresis and Noise margin.

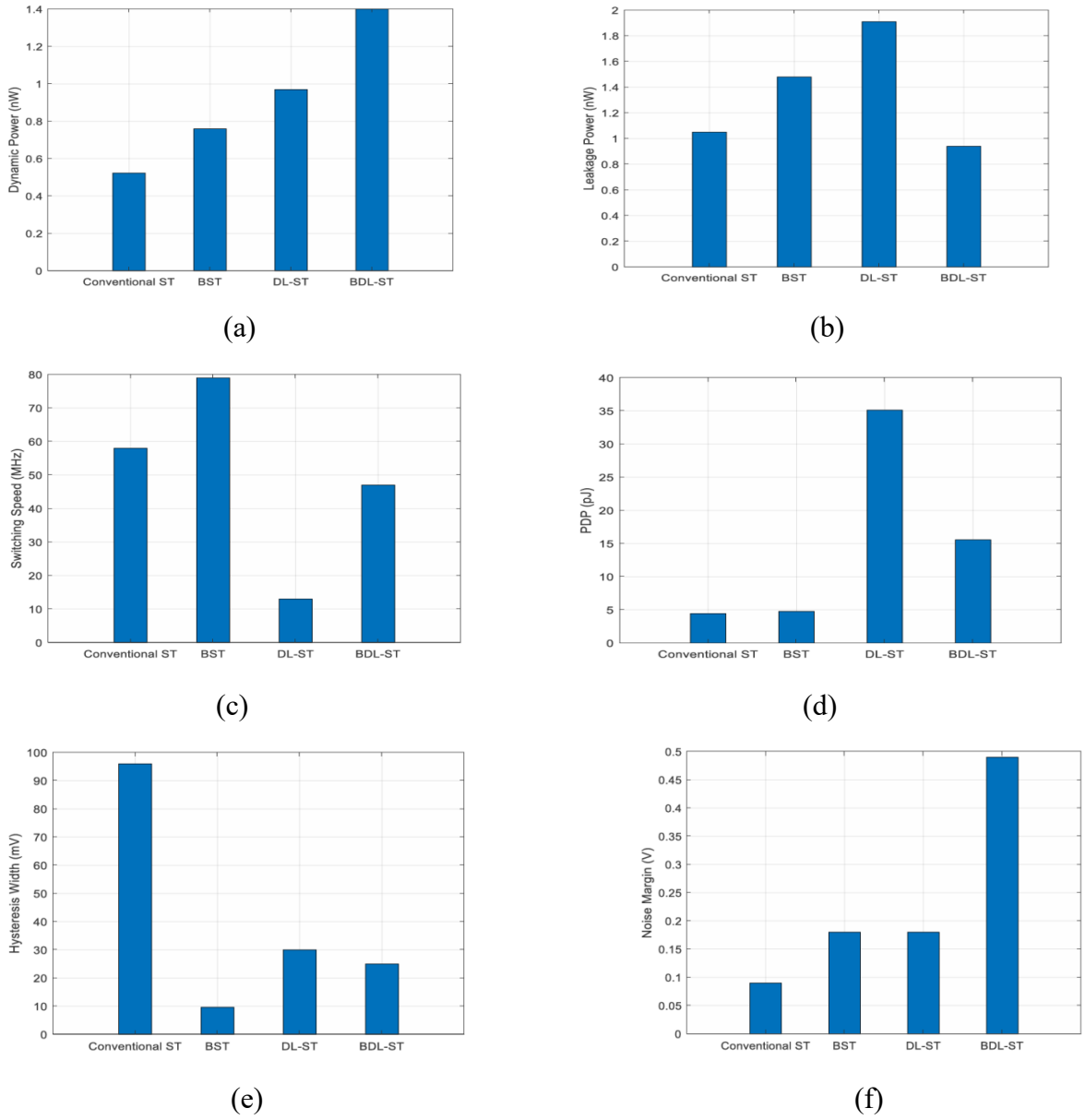

Fig.6. Performance analysis of various Schmitt trigger topologies: (a) Dynamic power (b) Leakage power (c) Switching peed (d) Power delay product (PDP) (e) Hysteresis width and (f) Noise margin.

As illustrated in Fig.6 (a), the Conventional ST has the lowest level of dynamic power due to being a static CMOS circuit. The dynamic power for both the BST and DL-ST is increased

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due to the increased capacitive coupling effects of the capacitive bootstrap and the dynamic nature of the clocked logic for the DL-ST, respectively. The new proposed BDL-ST has the highest level of dynamic power primarily due to the combination of domino evaluation logic and the charging effect of the capacitive bootstrap.

The BDL-ST has the lowest level of leakage power of the reviewed architectures as shown in Fig.6(b), indicating that BDL-ST succeeds in suppressing subthreshold leakage through a combination of transistor stacking and controlled evaluation paths.

The highest switching speed is provided by the BST since bootstrapping increases the effective gate overdrive. The DL-ST has a significant speed penalty due to keeper contention and charge sharing. However, in Fig.6(c) is clearly evident that the proposed BDL-ST greatly increases the switching speed over the DL-ST, indicating that bootstrapping eliminates many of the delay penalties associated with domino logic circuits.

The conventional ST and BST both provide a low power delay product (PDP), while the DL-ST has a much higher PDP due to high delay and leakage. The proposed BDL-ST produces a much lower PDP than the DL-ST, confirming that it has higher energy efficiency than the DL-ST, as shown in Fig.6 (d).

From the Fig.6 (e), it can be seen that a conventional ST has the largest hysteresis, which gives it the best possible noise immunity, but this also restricts its ability to switch at low voltages. In contrast, the proposed BDL-ST has a moderate hysteresis, which offers a more balanced combination of noise immunity and switch sensitivity.

The noise margin analysis shows that the proposed BDL-ST also has higher levels of noise margin when compared with other technologies, indicating that it has the highest levels of robustness against varying levels of noise and supply voltage, as demonstrated by Fig.6 (f). The characteristics of the BDL-ST suggest it is an excellent compromise among speed, leakage power, energy efficiency, and noise robustness, and will be well suited for use in ultra-low power and noise-resilient digital applications.

5. CONCLUSION

The findings in this research illustrate that the use of a bootstrapped domino logic-based Schmitt trigger meets the needs for low power, noise immunity, and fast switching speed when using an 18nm FinFET technology based device. This was achieved through the utilisation of capacitive bootstrapping combined with dynamic domino logic. Therefore, if there is any interest in the use of this device for low voltage system applications then that will remove some of the limitations related to the typical Schmitt trigger designs. All simulations run using the cadent virtuoso environment show that the switching speed of the BDL-ST is significantly faster than other designs while reducing overall leakage power and increasing noise tolerance over similar designs. Further to the advantages identified above, the design

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supports operation in both high speed and noise tolerant modes allowing for maximum design flexibility. The low leakage currents, fast switching speed and excellent noise tolerance characteristics demonstrate that the proposed BDLST will be especially useful in the development of power systems and for always-on sensing applications in electrically noisy and energy-limited environments.

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